Advanced Engineered Substrates for the Integration of Lattice-Mismatched Materials with Silicon

by

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Submitted to the Department of Materials Science and Engineering
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ABSTRACT

The dramatic advances in Si/SiO_2-based microelectronic processing witnessed over the past several decades can largely be attributed to relatively material-independent device scaling. However, with physical and economic limitations to the continued scaling of such devices appearing on the horizon, it is likely that near-term advances will come from the integration of novel and previously underrepresented materials. One of the most promising ways to enhance performance comes from the integration of judiciously chosen lattice-mismatched materials with Si. However, the integration of such structures typically poses significant technical challenges. The work contained in this thesis seeks to address several of these important issues, primarily through the use of relaxed, graded SiGe buffers on Si (i.e. $\nabla_x[Si_{1-x}Ge_x]/Si$).

Several new phenomena in relaxed graded SiGe buffers are developed in this thesis. A rise in threading dislocation density was observed in high-Ge content relaxed graded SiGe layers grown at relatively high temperatures, which was attributed to dislocation nucleation. This observation is contrary to conventional graded buffer theory in which high growth temperatures are expected to result in reduced threading dislocation densities (TDDs). Additionally, a coupling effect between the effective strain and the growth rate was observed, as evidenced by increased TDD values at reduced growth rates. This observation is attributed to reduced growth rates allowing more time for the surface to evolve (i.e. roughen) during growth, thereby trapping mobile dislocations and necessitating the nucleation of additional dislocations to continue relaxing the structure.

Also detailed in this thesis is the creation of two novel CMOS-compatible platforms for high-power applications: strained-silicon on silicon (SSOS) and strained-silicon on silicon-germanium on silicon (SGOS). SSOS substrate has an epitaxially-defined, tensilely strained silicon (ε-Si) layer directly on bulk silicon wafer without an intermediate SiGe or oxide layer. SSOS is a homochemical heterojunction, i.e. a heterojunction defined by strain state only and not by an

accompanying compositional change, and therefore in principle SSOS may ease metal-oxide-semiconductor (MOS) ε-Si fabrication as SiGe is absent from the structure. SGOS has an epitaxially-defined SiGe layer between the strained silicon channel and the Si substrate, which is likely necessary to prevent excessive off-state leakage in MOS devices due to overlap of the source-drain contacts and the interfacial misfit array.

The thesis concludes with a study of utilizing buried ε-Si layers for improving the fabrication of SSOI substrate via the hydrogen induced layer exfoliation process. Previous work involving tensile ε-$Si_{0.4}Ge_{0.6}$ layers in relaxed $Ge/\nabla_x[Si_{1-x}Ge_x]/Si$ demonstrated that significant hydrogen gettering via the formation of strain-relieving platelets occurred within the tensile ε-$Si_{0.4}Ge_{0.6}$ layers, leading to an overall increase in layer transfer efficiency for GOI substrate fabrication. Buried tensile ε-Si layers in relaxed $Si_{1-x}Ge_x$ for SSOI fabrication, however, demonstrate markedly different hydrogen gettering behavior that is dependent on a combination of both the degree of tensile strain as well the amount of damage present in the adjacent $Si_{1-x}Ge_x$ alloy. It was determined that a tensile strain level of approximately 1.6% in Si (corresponding to a $Si_{0.6}Ge_{0.4}$-based donor structure) was needed to create sufficient engineered damage to overcome the implantation damage in the adjacent $Si_{0.6}Ge_{0.4}$ layers and result in enhanced layer exfoliation. Lastly, an advanced $Si_{0.6}Ge_{0.4}$-based structure which incorporated ε-Si layers as transfer, hydrogen gettering, and etchstop layers was demonstrated. Such a structure may prove useful for the reuse of significant portions of the original SSOI donor structure, thereby potentially speeding commercial adoption of the SSOI platform.

Thesis Supervisor: Eugene A. Fitzgerald
Title: Merton C. Flemings - SMA Professor of Materials Science and Engineering

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During my time in *Professor Eugene Fitzgerald's* group at MIT and as well as my time at IBM, I was able to work on every MOSFET component except one, the gate electrode. It is somewhat fitting that the one component I never worked one was the gate, as I was never held back from anything during my tenure in his group. Even early on in my time in the group, I was given me the freedom to explore a multitude of entirely different projects, often simultaneously. I am grateful for the opportunity to work in his group, as well as the opportunity to visit Singapore, Hawaii, and Tokyo (albeit clandestinely).

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[1] Prime example: his claim to have invented the question mark.
[2] I suspect this page will disappear from the library copy soon after it is put on the shelf.

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[3] Subject to change.

CHAPTER 1: INTRODUCTION

"Pretend for a moment that I don't know anything about metallurgy, engineering, or physics, and just tell me what the hell is going on."

- Dr. Peter Venkman

1.1 MOORE'S FIRST LAW AND THE INEVITABLE END OF TRADITIONAL METAL-OXIDE-SEMICONDUCTOR DEVICE SCALING

Born in the late 1950s and having since grown into an industry with annual revenues currently in excess of $200 billion, the modern Si-based semiconductor microelectronics industry is, quite simply, an amazing technical and financial accomplishment. With its extremely robust oxide, relatively low cost, and ready availability in large diameter substrates (currently processed in leading-edge CMOS foundries at 300mm diameter), Si has remained the unparalleled material of choice for complementary metal-oxide-semiconductor (CMOS) devices.

The Si/SiO_2 material combination has been of such unequaled quality that it has almost entirely allowed the process of geometrical scaling, rather than the introduction of novel materials, to provide for the increased performance of CMOS devices. This was originally predicted in the form of Moore's Law, which stated that transistor density would double every 18-24 months for the foreseeable future. (*1*)

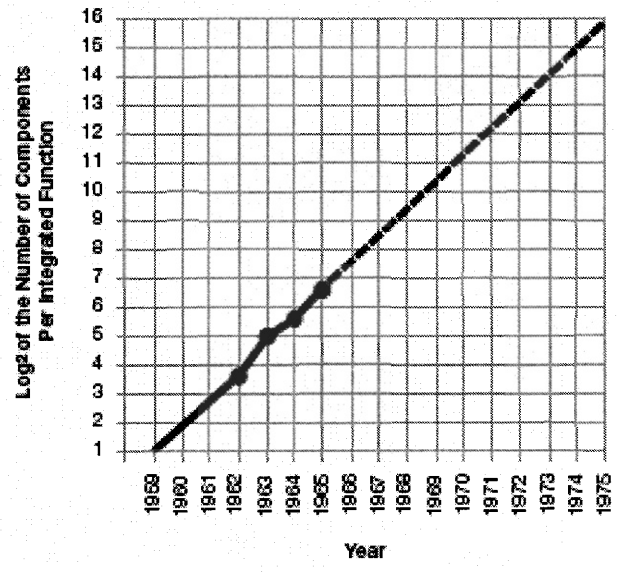


FIGURE 1.1 – Plot of the $\log_2$ of the number of components per integrated function as a function of time in the early years of the integrated circuit industry. The trend has continued well beyond 1975. (*1*)

The trend exhibited in **Figure 1.1** is simply phenomenal. At present, the 65 nm node is going into production, with the next generation 45nm node scheduled to be released in late 2007 or 2008. (*2*) Unfortunately, however, the increased transistor density predicted by Gordon Moore in 1965 has important limitations, as it is becoming increasing expensive to continue to pack additional transistors into the same space. In the words of Gordon Moore himself, "Capital costs are rising far faster than revenue", and as a result, "the rate of technological progress is going to be controlled [by] financial realities". (*3*) This latter statement has been subsequently dubbed "Moore's Second Law".

1.2 MOORE'S SECOND LAW AND THE NEED FOR THE INTEGRATION OF NEW MATERIALS

The end of Moore's Law has been claimed several times. The author makes no claim here to take an alarmist view and predict the end of traditional scaling in the immediate future. Gordon Moore himself said in 2003 that "another decade is probably straightforward...there is certainly no end to creativity." (*4*) However, it is indisputable that device dimensions cannot continue to scale indefinitely. Quite simply, as the physical dimensions of Si-based CMOS devices become increasingly smaller and approach atomic dimensions, devices will rapidly approach physical and economic limits.

If the basic structure of existing device architectures is to be retained, it will almost certainly prove imperative that future CMOS generations employ novel materials with superior properties relative to bulk Si. This will result in the possibility for enhanced performance through the use of materials such as SiGe and strained-Si (ε-Si), as well as other alternate paths to traditional scaling such as the use of engineered substrates, as shown in **Figure 1.2**.

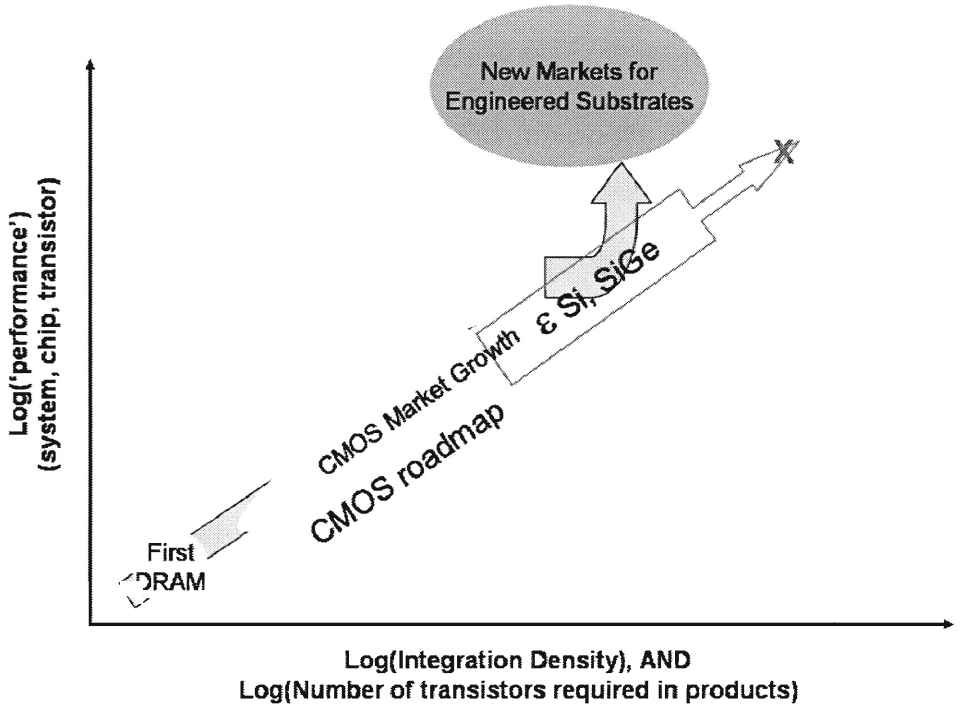


FIGURE 1.2 – Extensions and alternate paths to Moore's Law using novel material combinations.

One of several key properties for device performance is the charge carrier mobility, as higher effective carrier mobility (μ_{eff}) values directly translate into decreased power consumption and higher drive currents (I_D) , as given by (*5*)

$$I_D = \frac{W}{L_{Gate}} \mu_{eff} C_{ox} (V_{GS} - V_T) V_{DS} \qquad [1.1]$$

The room temperature carrier mobility values of bulk Si, Ge, and GaAs are presented in **Table 1.1.** (*6, 7*)

Table 1.1 – Electron and hole mobility values of bulk Si[6], Ge[6], and GaAs[7]

Material	Electron Mobility [$cm^2 V^{-1} s^{-1}$]	Hole Mobility [$cm^2 V^{-1} s^{-1}$]
Si	1450	450
Ge	3900	1900
GaAs	8500	400

Thus, it can be seen that Ge has significantly enhanced electron and hole mobility values relative to Si, while GaAs has a significantly enhanced electron mobility value relative to Si. However, one significant advantage that GaAs has over both Si and Ge for optoelectronic applications is its direct energy bandgap, which allows it to efficiently absorb and emit light. In contrast, Si and Ge are both indirect bandgap semiconductors, in that while they can absorb light fairly well, they are impractical as the active component in devices which emit light. Successful integration of direct bandgap materials with Si would allow for optoelectronic and microelectronic devices on the same platform, thus enabling increased device functionality and performance. Shown in **Figure 1.3** is a plot of the energy bandgap values of various semiconductor materials as a function of their lattice constant.

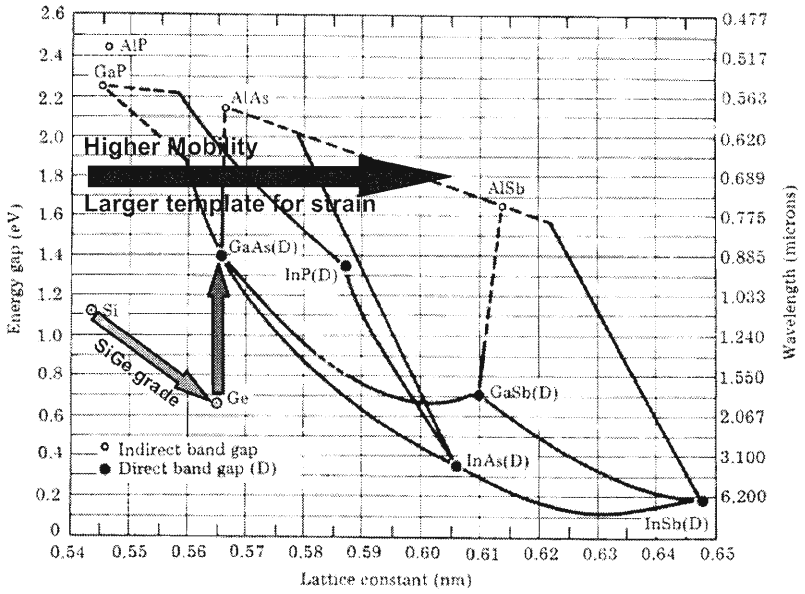


FIGURE 1.3 – The lattice constant vs. energy gap diagram for column IV and III-V semiconductor materials. Adapted from Mayer and Lau. (7)

As can be seen in **Figure 1.3**, many semiconductors known to have enhanced optoelectronic and carrier transport properties relative to Si, such as Ge, GaAs and InP, have lattice constants larger than Si. The integration of such materials with low-cost, large diameter Si substrates would therefore allow for a

tremendous advancement in modern microelectronics not through continued scaling advancements, but rather at the material level. Unfortunately, as will be discussed in further detail in subsequent chapters, the successful integration of these materials can be exceedingly difficult without introducing significant levels of deleterious, performance reducing defects.

To date, the key enabling technology for the integration of high-quality, lattice-mismatched materials involves the relaxed graded buffer. (*8, 9*) This method employs growing a series of layers with varying composition, such that the gap in lattice constant between two semiconductor materials is slowly bridged. As shown in **Figure 1.3**, for example, growth of SiGe alloys with increasing Ge concentration could be employed to attain the lattice constant of Ge on Si. GaAs-based devices could then be fabricated on this platform owing to the close lattice match between Ge and GaAs. The relaxed graded buffer concept has been successfully demonstrated using several materials systems, including SiGe on Si(001) substrates (i.e. $\nabla_x[Si_{1-x}Ge_x]/Si$) (*8, 9*), InGaP on GaP substrates (i.e. $\nabla_y[In_yGa_{1-y}P]/GaP$) (*10*), and InGaAs on GaAs substrates (i.e. $\nabla_z[In_zGa_{1-z}As]/GaAs$). (*11, 12*)

1.3 SCOPE AND ORGANIZATION OF THESIS

The work entailed within this thesis studies various methods to improve the integration of lattice-mismatched materials with Si in a broad range of ways. As will be seen, a common thread running through every component of this thesis is the relaxed graded SiGe buffer ($\nabla_x[Si_{1-x}Ge_x]/Si$) platform.

Chapter 2 provides a broad overview of the state of knowledge regarding lattice-mismatched epitaxy prior to this work. Included also is a discussion of the growth of mismatched layers via the deposition of both uniform single layers as well as relaxed graded buffer layers.

Chapter 3 contains background information on the growth of the $\nabla_x[Si_{1-x}Ge_x]/Si$ platform, as well as details on the subsequent growth of strained ε-$Si_{1-y}Ge_y$ heterostructures and GaAs on this platform. Finally, the characterization methods employed for the experimental structures utilized in this work are described in detail.

Chapter 4 further explores the model for the accommodation of applied mismatch strain in relaxed graded buffers briefly introduced in **Chapter 2**. The focus of this work is on the control of threading dislocations during growth, both by the suppression of the nucleation of additional dislocations as well as by maximizing the glide efficiency of pre-existing dislocations. The chapter develops a framework for obtaining a high-quality GaAs on Si platform, consisting of GaAs on $Si_{0.04}Ge_{0.96}/\nabla_x[Si_{1-x}Ge_x]/Si$.

Chapter 5 introduces relaxed buffer bonding, a central topic for the remainder of the thesis. Relaxed buffer bonding involves the growth of a relaxed graded semiconductor in order to obtain a low defect density substrate of arbitrary surface lattice constant. A general transfer structure, possibly consisting of strained and/or etchstop layers, is then grown at low temperatures atop this relaxed graded structure. The uppermost layer(s) are then bonded and transferred to another substrate, typically referred to as the handle substrate. Examples of various existing structures fabricated using this method are discussed.

Chapter 6 describes the fabrication of several novel CMOS-compatible semiconductor structures for high-power applications. The chapter describes the self-heating effect, in which Joule heating results in a significant temperature increase and concomitant reduction in carrier mobility in the active region of the device. Two novel solutions to the self-heating problem are offered for strained Si-based applications. The first involves the transfer of a strained Si layer directly to a Si handle substrate, a structure known as strained silicon-on-silicon (SSOS).

The second involves the transfer of a strained Si layer with a thin overlayer of relaxed SiGe to another Si handle wafer. Both platforms are expected to demonstrate significantly enhanced thermal conductivity near the active region of the device relative to strained-Si on a thick, relaxed SiGe buffer.

Chapter 7 investigates several approaches for improving the fabrication of strained silicon-on-insulator (SSOI), strained silicon-on-silicon (SSOS), and silicon germanium-on-silicon (SGOS) substrates. Specifically, the use of buried tensilely-strained Si layers is investigated for potentially using such layers for increasing the transfer efficiency of H-implanted structures. Additionally, the use of buried strained-Si layers is explored for potentially reusing a significant portion of the SiGe graded buffer donor structure.

Finally, **Chapter 8** summarizes the major results of the thesis and suggests directions for future work.

CHAPTER 2: INTEGRATION OF LATTICE-MISMATCHED SEMICONDUCTORS WITH SI

"There's something very important I forgot to tell you."

- Dr. Egon Spengler

2.1 INTRODUCTION

Within the last two decades, three key advances have occurred in the field of heteroepitaxy which allow for the integration of high-quality, lattice-mismatched materials with Si. Specifically, these advances include:

1. the development of the relaxed graded buffer, which can provide an arbitrary lattice constant with a low defect density.
2. the development of highly strained layers ($|\varepsilon| \geq$ 1-2%) on relaxed graded buffers.
3. the transferal of strained and relaxed epitaxial layers to other substrates.

A brief introduction to the first two advances will be provided in the current chapter, with more in-depth treatments to follow in subsequent chapters. Layer transfer from relaxed SiGe buffers, a process known as relaxed buffer bonding, will be treated in detail in **Chapter 5**.

2.2 FUNDAMENTALS OF LATTICE-MISMATCHED EPITAXY

Epitaxial growth of lattice-mismatched material typically proceeds as shown in **Figure 2.1**. In the case shown, the lattice constant of the film is greater than that of the substrate, as is generally the case for graded structures. For thin films, the applied mismatch strain is initially accommodated elastically, such that the in-plane lattice constant of the film conforms to that of the host substrate, yet the out-of-plane lattice constant is significantly extended as shown in **Figure 2.1(a)**. For this case, the film is tetragonally-distorted but remains coherent with the substrate, and as growth proceeds strain is continually added to the film. If sufficient strain is applied, misfit dislocations will appear at the heterointerface to partially relieve this strain, as shown in **Figure 2.1(b)**, and the film can thereby "relax" in order to approach its equilibrium lattice constant.

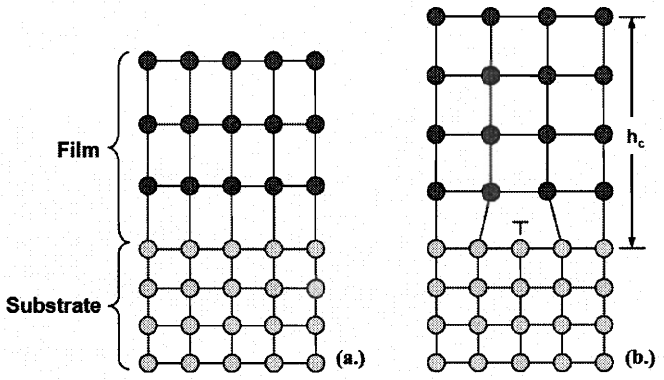


FIGURE 2.1 – Schematics of (a) a coherently strained film and (b) a partially-relaxed film. Note the out-of-plane tetragonal distortion in (a) associated with the retention of compressive elastic strain. Image courtesy of A. J. Pitera. (*13*)

The thickness at which it becomes thermodynamically possible to introduce dislocations is termed the critical thickness, h_c, and depends upon the material properties and the degree of strain application as

$$h_c = \frac{G_o G_s (1 - \nu \cos^2 \alpha)(b / b_{eff})}{2\pi (G_o + G_s)(1 - \nu) Y_o f} \ln\left(\frac{h_c}{b}\right) \qquad \textbf{[2.1]}$$

where b and b_{eff} are the full and effective Burgers vectors of the dislocation, v is Poisson's ratio, G_o and Y_o are the shear and elastic moduli of the film, respectively, G_s is the shear modulus of the substrate, α is the angle between the Burgers vector and the dislocation line, and f is the degree of mismatch strain is applied to the film. (*14*) Thus, an increase in the applied mismatch strain results in a reduction of the critical thickness, as expected.

In general, the ease with which dissimilar materials can be successfully integrated is largely dependent upon the lattice mismatch, f, which is geometrically determined by the lattice parameters of the film and substrate as

$$f = \frac{a_{sub} - a_{film}}{a_{film}} \qquad [2.2]$$

where a_{film} and a_{sub} are the lattice constants of the film and the substrate, respectively. For high-mismatch films, i.e. those with f > 0.015-0.02, relaxation will occur via the rampant nucleation of a large number of threading dislocations with short misfit dislocation segments. The threading dislocation density in such films is typically greater than 10^8 cm^{-2}, a level considerably higher than that tolerable by most devices.

In contrast, in low-mismatch films, i.e. for those with f < 0.01, relaxation occurs with a low density of threading dislocations with long misfit dislocation segments. This is fortuitous, as low threading dislocation levels are typically required for most practical applications, and therefore the remainder of this work will focus on this technologically significant regime of epitaxial growth. Schematics of these cases are presented in **Figure 2.2**.

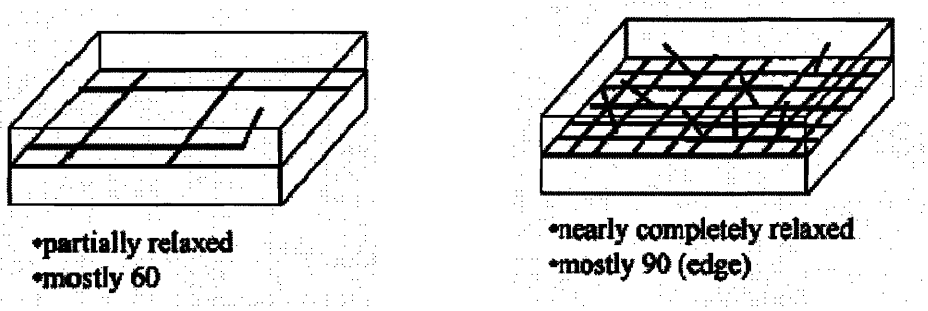


FIGURE 2.2 – Schematics of the relaxation of (a) a single layer with low lattice-mismatch and (b) a single layer with high lattice-mismatch.

The exact mechanism by which dislocations relieve strain in low-lattice mismatch systems (i.e. <1% mismatch strain) is well understood. Under sufficient applied strain, dislocations in diamond-cubic and zinc-blended semiconductors will propagate on {111} planes along [110] directions, as shown in **Figure 2.3**. As

the dislocation density of most current semiconductor substrates is negligible compared to those required for relaxation, the most likely operative mode for relaxation via dislocation motion is through the nucleation of half-loops originating from sources at the surface and propagating towards the mismatched interface. In this way, 60° threading dislocations continue to glide along the aforementioned glide system to form strain-relieving misfit dislocations with effective Burgers vector

$$b_{eff} = \frac{|\vec{b}|}{2} = \frac{\sqrt{2}a}{4} \qquad \textbf{[2.3]}$$

where *a* is the lattice constant of the layer. The effective Burgers vector, b_{eff} is reduced by a factor of 2 relative to the full Burgers vector, $\vec{b}$, in these systems as 60° dislocations are only half as efficient at relieving strain as full edge dislocations. Fortunately, however, in such low lattice-mismatch systems both dislocation nucleation as well as dislocation-dislocation interactions are suppressed, thereby allowing for efficient strain relief with a low threading dislocation density. It should be stressed that the application of this approach alone has little inherent value, as for most applications little is gained by increasing the lattice constant by such a small amount.

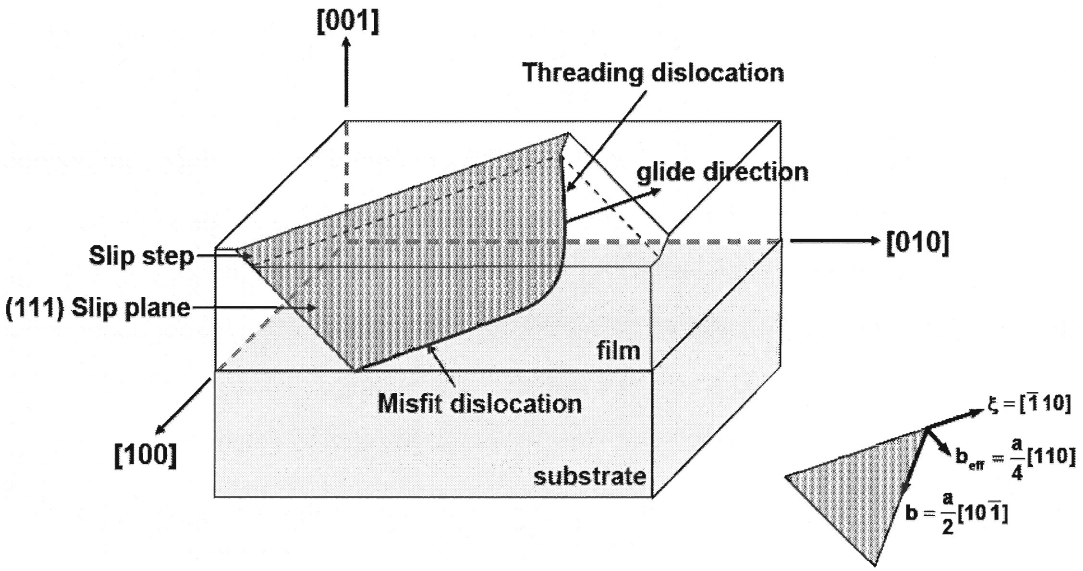


FIGURE 2.3 – Schematic of threading and misfit dislocations in a partially-relaxed lattice-mismatched layer grown beyond the critical thickness. Image courtesy of A. J. Pitera. (*13*)

The key development in the integration of materials with significantly different lattice constants via epitaxial growth was to extend the above approach by slowly relieving significant amounts of strain via the growth of a *series* of low lattice-mismatch layers, such that at no time during the growth process are large amounts of strain ever applied to the system. (*8, 9*) To date, only this technique, dubbed the relaxed graded buffer, has allowed for the attainment of large differences in lattice constant relative to the original substrate with low dislocation densities via epitaxy.

2.3 RELAXED GRADED BUFFER LAYERS

The thickness at which it becomes thermodynamically possible to introduce dislocations in graded buffers is modified from that of a uniform mismatched layer undergoing relaxation. The critical thickness for graded buffers, $h_{c,buffer}$, depends upon the material properties and the rate of strain application as

$$h_{c,buffer}^2 = \frac{3Gb\left(1-\frac{\nu}{4}\right)\ln\left(\frac{eh_c}{b}\right)}{2\pi(1-\nu)YC_f} \qquad \textbf{[2.4]}$$

where b is the Burgers vector of the dislocation, v is Poisson's ratio, G and Y are the shear and elastic moduli of the film, respectively, and C_f is the rate at which mismatch strain is applied to the film. (*9*) Thus, an increase in the applied strain rate results in a reduction of the critical thickness, as expected.

The dependence of the threading dislocation density (TDD), ρ, on the various growth parameters for relaxed graded buffers has been shown to be:

$$\rho = \frac{2R_g R_{gr} \exp\left(\frac{E_{glide}}{kT}\right)}{bBY^m \varepsilon_{eff}^m} \qquad \textbf{[2.5]}$$

where R_g and R_{gr} are the growth and compositional grading rates, respectively, m is an exponent with a value generally between 1 and 2, B is a constant, T is the temperature, Y is the modulus, k is Boltzmann's constant, E_{glide} is the activation energy for dislocation glide, and b is the Burger's vector magnitude and the dislocations are assumed to be 60° dislocations. (*15*) To date, the most fruitful work on reducing the TDD in SiGe graded buffers has centered on increasing the growth temperature, thereby increasing the glide velocity and, hence, relaxation efficiency by reducing the equilibrium density of dislocations required to relax the film. Furthermore, a key factor in keeping the threading dislocation density low in relaxed graded buffers is the fact that threading dislocations can be effectively "recycled" from one layer to the next. In this way, a single threading dislocation can contribute strain-relieving misfit dislocation segments across multiple interfaces. A schematic and cross-sectional transmission electron microscopy (XTEM) micrograph of a relaxed graded SiGe buffer are shown in **Figure 2.4**.

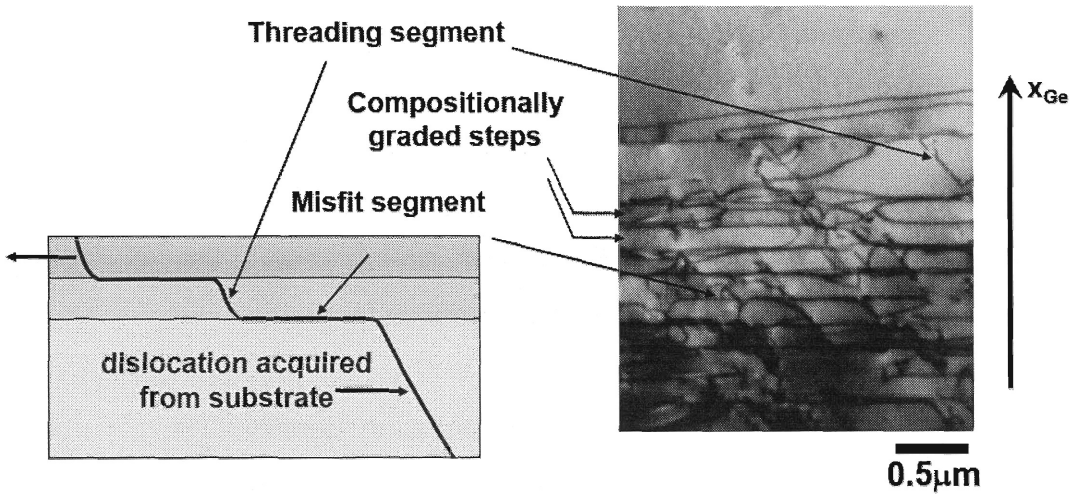


FIGURE 2.4 – (a) Schematic and (b) cross-sectional transmission electron microscopy micrograph of the process by which individual threading dislocations can utilized to facilitate the relaxation of multiple layers. Image courtesy of A. J. Pitera. (*13*)

The relaxed graded buffer concept has been successfully demonstrated using several materials systems. Examples of such structures include relaxed graded SiGe on Si(001) substrates (i.e. $\nabla_x[Si_{1-x}Ge_x]/Si$) (*8, 9*), InGaP on GaP substrates (i.e. $\nabla_y[In_yGa_{1-y}P]/GaP$) (*10*), and InGaAs on GaAs substrates (i.e. $\nabla_z[In_zGa_{1-z}As]/GaAs$) (*11, 12*). In particular, the $\nabla_x[Si_{1-x}Ge_x]/Si$ structure has proven enormously successful for the fabrication of high-mobility strained-Si and strained-Ge devices (*16-21*), as well as the $Ge/\nabla_x[Si_{1-x}Ge_x]/Si$ platform for the subsequent growth of III-V devices such as lasers (*22, 23*), waveguides (*24*), and high-efficiency solar cells. (*25-27*) In this system, scaleable $\nabla_x[Si_{1-x}Ge_x]/Si$ structures with dislocation densities on the order of 10^5 to 10^6 cm^{-2} can be fabricated across the entire composition range. (*28*)

2.4 ε-$Si_{1-y}Ge_y$ HETEROSTRUCTURES ON $\nabla_x[Si_{1-x}Ge_x]/Si$

As mentioned earlier in this chapter, the second key development in the heteroepitaxial growth of lattice mismatched layers to occur in the last 2 decades involves the growth of highly strained films, i.e. $|\varepsilon| \geq 1$-2%. The earliest work in this field involved the growth of thin, tensilely strained Si layers on relaxed graded $Si_{1-x}Ge_x$. Such ε-Si layers exhibited improvements in both electron and hole carrier mobilities, with more enhancement in the former. As such, this "single-channel" structure was particularly useful for enhanced NMOS performance. (*8*) An XTEM micrograph of a ε-Si/$Si_{0.8}Ge_{0.2}$ single-channel heterostructure is shown in **Figure 2.5**.

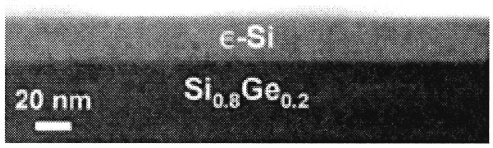


FIGURE 2.5 – Cross-sectional transmission electron microscopy micrograph of a "single-channel" ε-Si layer on relaxed $Si_{0.8}Ge_{0.2}$. Image courtesy of M. L. Lee. (*29*)

However, it was soon demonstrated that compressively strained $Si_{1-y}Ge_y$ layers on relaxed $Si_{1-x}Ge_x$ (i.e. y>x) exhibited enhanced hole mobility values relative to bulk Si. (*20*) A natural extension, therefore, was to incorporate both tensilely strained Si layers and compressively strained $Si_{1-y}Ge_y$ layers on the same $\nabla_x[Si_{1-x}Ge_x]/Si$ platform. This "dual-channel" structure could then be utilized for both NMOS and PMOS devices. Strain engineering thereby provides the ability to tailor the transport properties of each layer to the extent that even symmetric electron and hole mobility values demonstrated. (*29*) An XTEM micrograph of a ε-Si/ε-Ge/$Si_{0.5}Ge_{0.5}$ dual-channel heterostructure is shown in **Figure 2.6**.

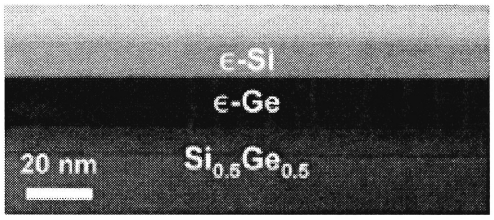


FIGURE 2.6 – Cross-sectional transmission electron microscopy micrograph of a "dual-channel" ε-Si/ε-Ge structure on relaxed $Si_{0.5}Ge_{0.5}$. Image courtesy of M. L. Lee. (*29*)

While the ε-Si/ε-Ge/$Si_{0.5}Ge_{0.5}$ dual-channel structure exhibits a significant performance enhancement over bulk Si, under certain processing conditions diffusion considerations necessitate the presence of an additional ε-Si layer to fully "clad" the compressively strained $Si_{1-y}Ge_y$ layer. The resulting "tri-layer" structure is therefore expected to offer the same performance enhancement of the dual-channel structure, but with significantly enhanced thermal stability under certain conditions. (*30, 31*) An XTEM micrograph of a ε-Si/ε-$Si_{0.5}Ge_{0.5}$/ε-Si/$Si_{0.8}Ge_{0.2}$ tri-layer heterostructure is shown in **Figure 2.7**.

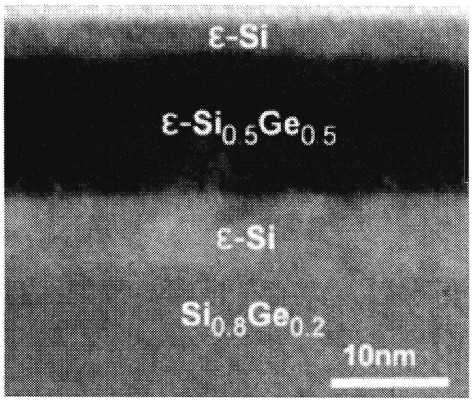


FIGURE 2.7 – Cross-sectional transmission electron microscopy micrograph of a "tri-layer" ε-Si/ε-$Si_{0.5}Ge_{0.5}$/ε-Si on relaxed $Si_{0.8}Ge_{0.2}$ (y>x). Image courtesy of S. Gupta. (*30, 31*)

2.5 GaAs-BASED HETEROSTRUCTURES ON $\nabla_x[Si_{1-x}Ge_x]/Si$

Direct growth of GaAs on Si results in dislocation densities on the order of 10^8-10^9 cm^{-2}, a level which is orders of magnitude higher than that tolerable by most devices. The approximate upper limits in threading dislocation density tolerable by various III-V devices are presented in Table 2.1, which clearly show that the direct growth of GaAs/Si results in material quality that is insufficient for the fabrication of reliable devices.

Table 2.1 – Approximate upper TDD limit for various III-V devices

Device	Max TDD [cm^{-2}]
FET	10^7
LED	10^6
Solar cell	10^6
Laser	10^5

While direct GaAs/Si growth is not an option for most devices, the TDD levels provided by the relaxed graded SiGe buffer approach are either within or very near to the necessary levels for proper performance of many III-V devices. In particular, TDD levels required for efficient GaAs-based solar cells are very near current Ge/$\nabla_x[Si_{1-x}Ge_x]$/Si TDD values (*32*), and a record minority-carrier lifetime of 10 ns for GaAs/Ge/$\nabla_x[Si_{1-x}Ge_x]$/Si has been reported. (*27*)

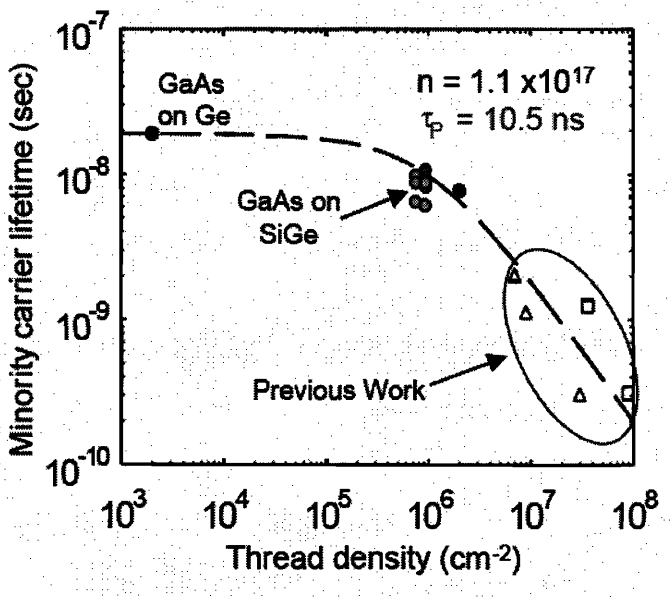


FIGURE 2.8 – Minority carrier lifetimes of GaAs films on Si compared to the calculated curve for low-doped GaAs. The minority carrier lifetime of GaAs grown on $Ge/\nabla_x[Si_{1-x}Ge_x]/Si$ is much higher than any previously reported. Image adapted from (*32, 33*).

As can clearly be seen in **Table 2.1**, the III-V device type that is most sensitive to the TDD level is the laser, making it an excellent test of material quality. AlGaAs/GaAs-based laser heterostructures were fabricated on our group's $Ge/\nabla_x[Si_{1-x}Ge_x]/Si$ platform, a cross-sectional TEM micrograph of which is shown in **Figure 2.9**. (*23*)

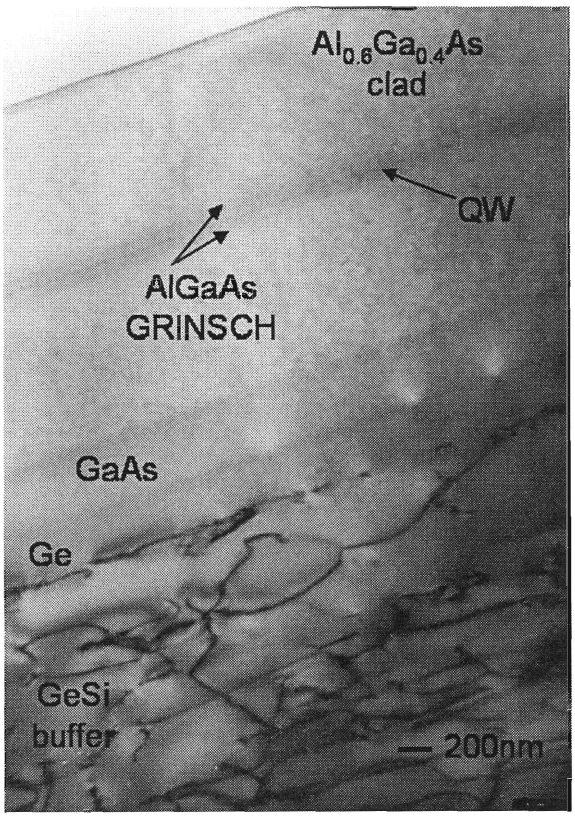


FIGURE 2.9 – XTEM micrograph of a III-V based laser structure on $Ge/\nabla_x[Si_{1-x}Ge_x]/Si$. Processed lasers had cavity lengths of 1.0–0.7 mm and oxide stripe widths of 5–20 mm. Image courtesy of M. E. Groenert *et al.* (*23*)

The performance characteristics of the above structure are presented in **Figure 2.10**. For comparison purposes, the above AlGaAs/GaAs heterostructure was fabricated both on both our group's $Ge/\nabla_x[Si_{1-x}Ge_x]/Si$ platform as well as a GaAs substrate which served as a control. As can be seen in **Figure 2.10**, there remains much work to be done in order to create reliable lasers on Si with identical performance to structures grown on GaAs substrate. However, as lasers are the most ambitious device from a defect-sensitivity standpoint, the work of Groenert *et al.* (*22, 23*) is highly encouraging.

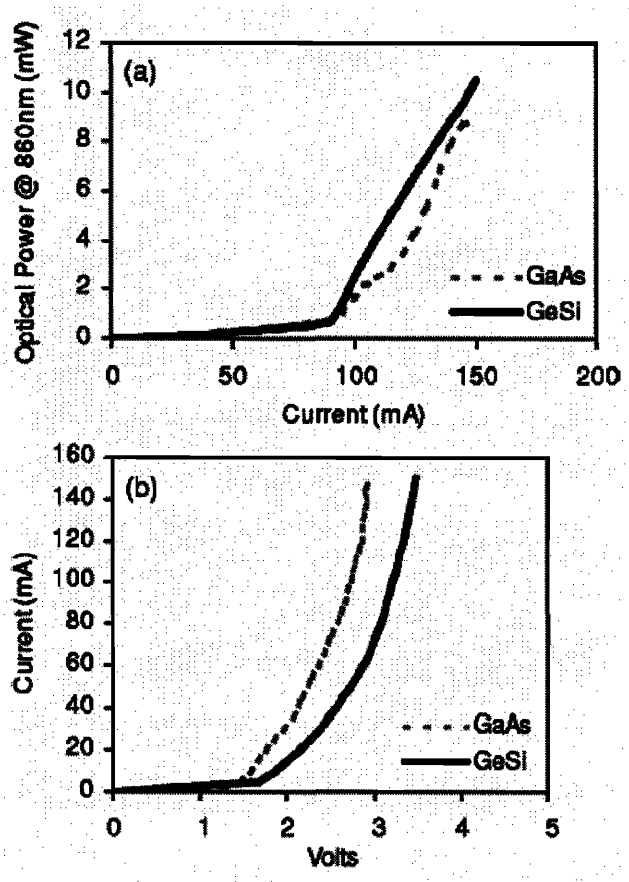


FIGURE 2.10 – (a) Side-by-side light vs. current and (b) current vs. voltage characteristics for identical GaAs/AlGaAs GRIN-SCH QW lasers grown on $Ge/\nabla_x[Si_{1-x}Ge_x]/Si$ and GaAs substrates. Images courtesy of M. E. Groenert *et al.* (*23*)

2.6 CONCLUSION

The concepts described in this chapter have allowed for significant advancements in CMOS performance as well as for the monolithic integration of optoelectronic III-V devices of unprecedented quality on Si. However, as will be discussed in **Chapter 4**, there are several conditions under which the theoretical underpinnings of the graded buffer approach fail. Additionally, as will be discussed in more detail in **Chapters 5-7**, there is currently a significant emphasis on the development of advanced engineered substrates in which the structures described in the present chapter are transferred to directly to silicon

wafers, thereby eliminating the SiGe relaxed graded buffer from the final structure.

CHAPTER 3: GaAs/Ge/ε-SiGe on $\nabla_x[Si_{1-x}Ge_x]$/Si Growth and Characterization

"You know, it just occurred to me that we really haven't had a successful test of this equipment."

- Dr. Ray Stantz

3.1 INTRODUCTION

This chapter provides an overview of the experimental techniques that are used throughout this thesis. The chapter begins with a general description of ultra-high vacuum chemical vapor deposition (UHVCVD), followed by a description of the details regarding the growth of the strained and relaxed SiGe-based structures used for this thesis. The chapter then gives a brief description of metal-organic chemical vapor deposition (MOCVD), the growth technique employed for the growth of GaAs layers used for this work. Finally, the chapter concludes with a description of the various characterization techniques employed throughout this thesis.

3.2 ULTRA-HIGH VACUUM CHEMICAL VAPOR DEPOSITION OF $\nabla_x[Si_{1-x}Ge_x]/Si$

3.2.1 OVERVIEW OF UHVCVD

The ultra-high vacuum chemical vapor deposition (UHVCVD) technique was developed in the mid-1980s for depositing epitaxial Si film at reduced growth temperatures. (*34*) However, the primary advantages of the UHVCVD system used in this study are its ability to grow high quality compositionally graded SiGe buffers at high temperatures (700–900°C) and highly strained heterostructures at low temperatures (350–650°C), in combination with the fact that deposition can occur on many substrates simultaneously.

3.2.2 GROWTH OF RELAXED SIGE BUFFERS

The UHVCVD system used in this study employs SiH_4 and GeH_4 source gases for the deposition of SiGe films. Dopants are supplied via 1% B_2H_6 in H_2 and 1% PH_3 in H_2 gases. The dopant gases can be further diluted with either H_2

or Ar via two dilution stages. The UHVCVD reactor used in this work is a hot-walled, load-locked system with a quartz growth chamber. The growth chamber can accommodate up to ten 150mm diameter substrates and has a base pressure of less than 1×10^{-9} Torr at 750°C. This base pressure is achieved through the use of a novel differential pumping scheme between two o-rings at the base of the quartz tube. The growth temperature of the system can vary from 350°C to 900°C; the upper limit is set by devitrification of the quartz tube and cooling of the o-rings at the tube base, while the lower limit is set by the thermally-activated cracking of the source gases. Typical growth pressures for the structures in this work varied between 1mT and 30mT and were regulated by partially closing a gate valve over the reactor turbo pump, thereby decreasing its pumping efficiency. A schematic of the UHVCVD system employed in this study is presented in **Figure 3.1** below.

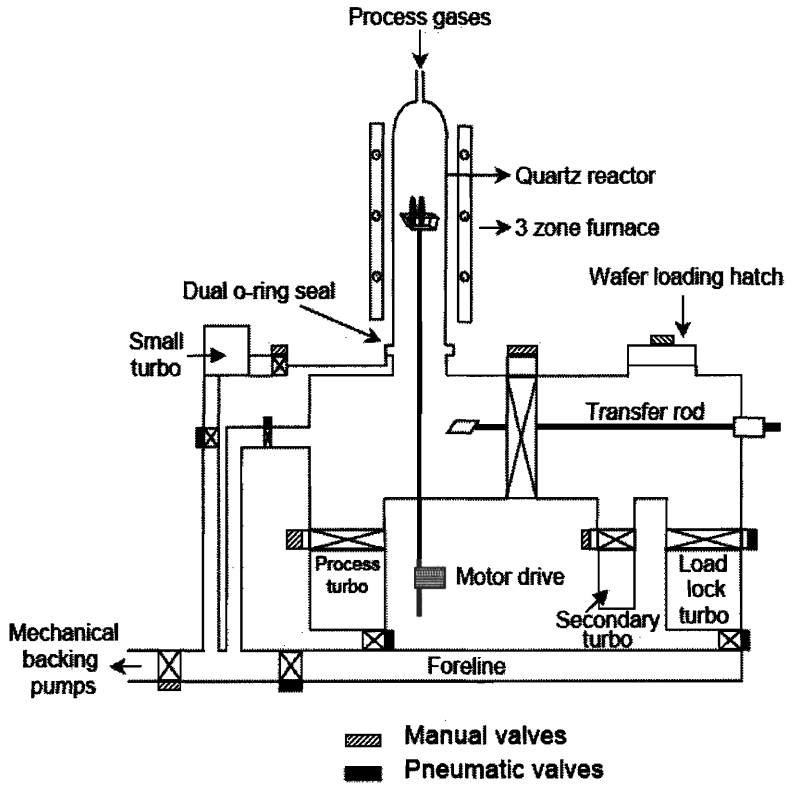


FIGURE 3.1 – Schematic of the UHVCVD system used in this work. Image courtesy of Samavedam *et al.* (*13, 33, 35-39*)

Prior to growth, Si wafers are typically subjected to a 10 minute piranha clean (3:1 H_2SO_4:H_2O_2) followed by a 1 minute HF dip (10:1 H_2O:HF), which yields a clean hydrogen-terminated surface. For regrowth on SiGe virtual substrates after an intermediate chemical-mechanical planarization (CMP) step, an analogous procedure is employed. However, following CMP, wafers are subjected to two piranha cleans instead of one (in an attempt to remove residual slurry contamination), with cleaning time reduced accordingly to avoid over-etching the SiGe layers. This is then followed by an HF dip that actually removes the slurry contamination. Wafers are then immediately loaded into the UHVCVD loadlock, which is pumped down for at least two hours. Prior to growth, the wafers are held under UHV conditions at roughly 200-250 °C for at least 30 minutes to desorb organics and adsorbed water. Finally, immediately prior to growth, wafers are subjected to a high-temperature desorption step (typically 900°C) to remove any remaining native oxide on the surface of the Si wafers. A 1 μm homoepitaxial buffer layer is then deposited to bury any residual impurities. Growth of SiGe layers then proceeds after homoepitaxial buffer growth. The carrier gas flow settings for $Si_{1-x}Ge_x$ for $x \leq 0.5$ are shown in **Figure 3.2**. In accordance with **Eqn. 2.5**, the growth temperature used for graded SiGe buffers in this composition range was 900 °C, the highest temperature possible with the UHVCVD system used in this study. Growth rates over this composition range were typically on the order of 7-10 Å s^{-1}, while the growth pressure was typically ~25 mTorr.

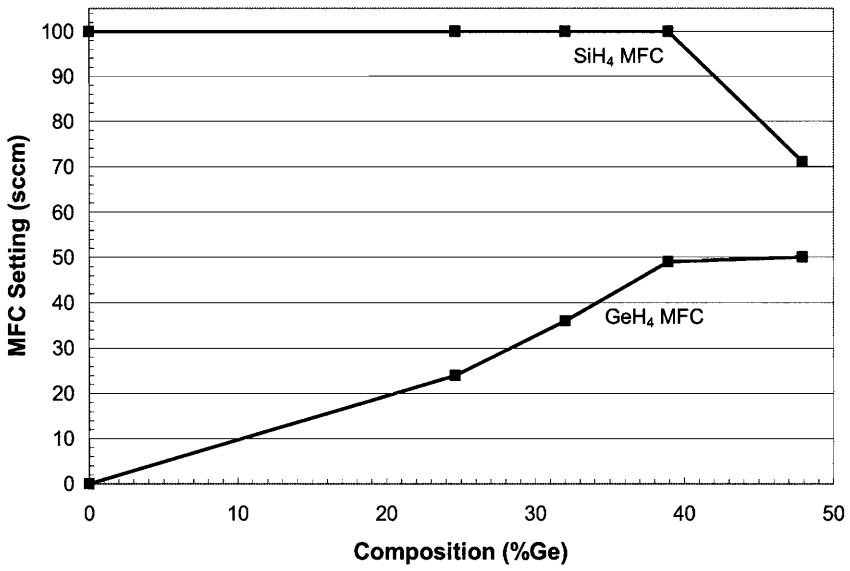


FIGURE 3.2 – Mass flow controller (MFC) settings for the growth of low-Ge content relaxed graded SiGe buffers using the UHVCVD system used in this work at 900 °C.

For the high-Ge content portion of the graded buffer, an attempt was made to determine the highest growth temperatures possible without the occurrence of gas phase nucleation (*40*) from the GeH_4 precursor gas used in this work. Shown in **Figure 3.3** are the results of this study, which show that the growth temperature can be successfully increased by 50-150 °C relative to previous reports by our group. (*41*) Growth rates were typically on the order of 3-8 Å s^{-1}, while the growth pressure was ~2-7 mTorr.

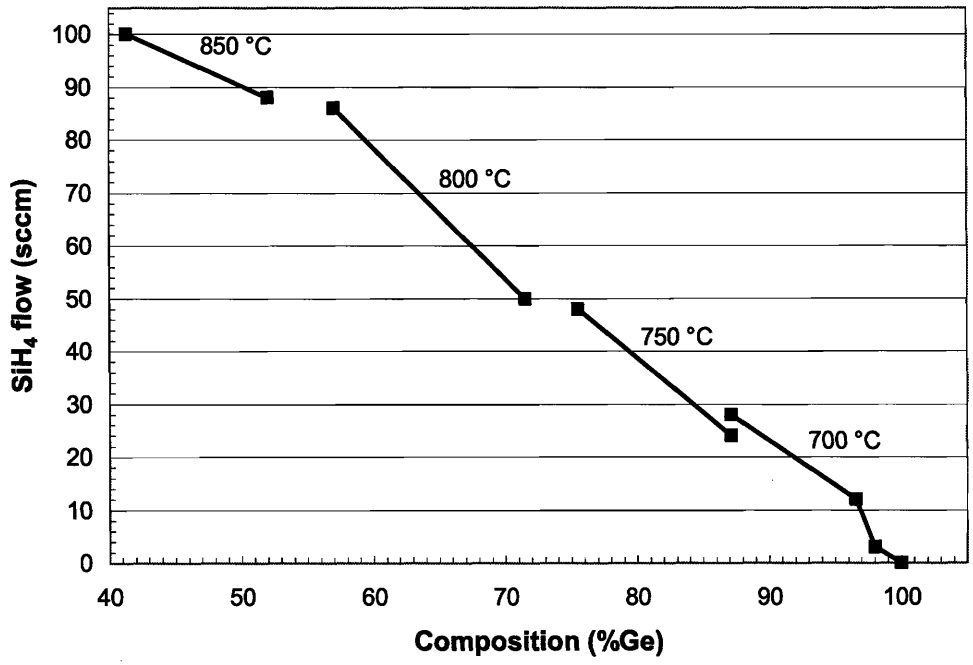


FIGURE 3.3 – Optimum temperature profile for the high-Ge content relaxed graded SiGe buffers using the UHVCVD system used in this work using high growth rates. The GeH_4 base flow was a constant 50 sccm.

Additionally, lower growth rates in the high-Ge content growth regime were investigated through the use of a reduced GeH_4 baseline flow, in this case 25 sccm. This was motivated by the growth rate dependence of the dislocation density expressed in **Eqn. 2.5**, which suggests that reduced growth rates, combined with high growth temperatures, should result in superior film quality. Shown in **Figure 3.4** are the results of this study. Growth rates with these gas flow settings were typically on the order of 1-4 Å s^{-1}, while the growth pressure was ~1-4 mTorr. It should be noted that the temperatures used in this study were identical to those used for the high growth rate calibration shown in **Figure 3.4**. However, as the occurrence of gas phase nucleation is dependent on both temperature and pressure, (*40*) the reduced pressures in this portion of the study would likely allow for slightly higher growth temperatures than those used here.

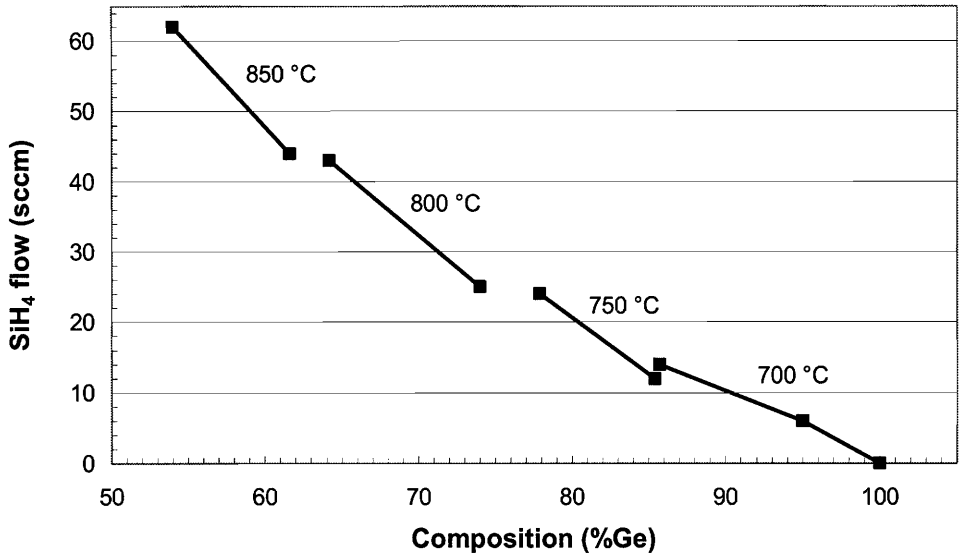


FIGURE 3.4 – Optimum temperature profile for high-Ge content relaxed graded SiGe buffers using the UHVCVD system used in this work using reduced growth rates. The GeH_4 base flow was a constant 25 sccm.

3.2.3 GROWTH OF ε-SIGE HETEROSTRUCTURES ON SIGE BUFFERS

In order to successfully fabricate the highly strained SiGe layers required for this thesis, reduced growth temperatures relative to those used for the growth of relaxed graded buffers were employed. For the strained heterostructures used in this work, a growth temperature of 550 °C was used. This growth temperature resulted in growth rates of approximately 0.1 Å s^{-1} for ε-Si and 2-2.5 Å s^{-1} for ε-$Si_{1-y}Ge_y$ layers of y~0.2-0.5. The increase in growth rate of more than an order of magnitude when GeH_4 is also present is due to the fact Ge acts to catalyze hydrogen desorption from the growth surface. (*42*) The GeH_4 flow settings for ε-$Si_{1-y}Ge_y$ films grown at 550 °C are shown in **Figure 3.5**.

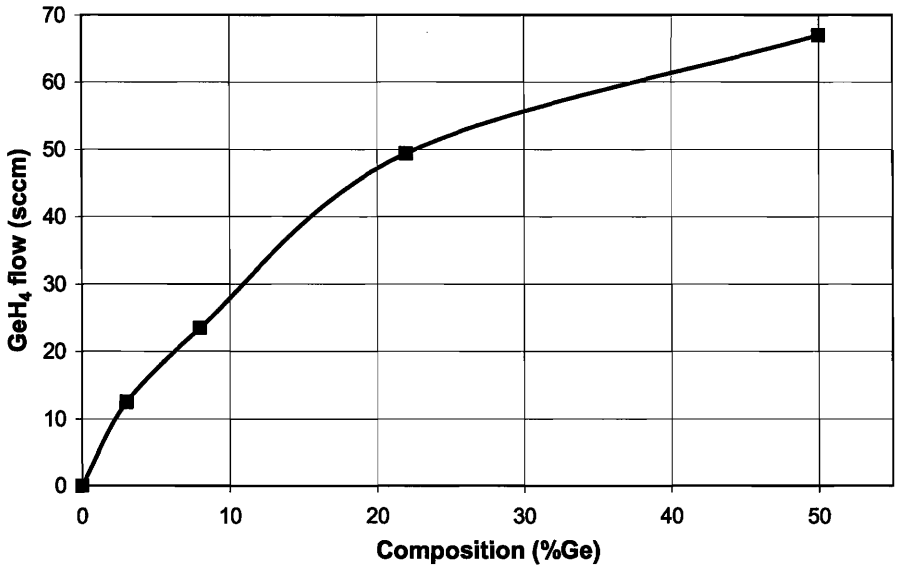


FIGURE 3.5 – SiGe compositions obtained in the UHVCVD system in this work as a function of GeH_4 flow at a growth temperature and pressure of 550°C and 2-4 mTorr, respectively.

3.3 METALLORGANIC CHEMICAL VAPOR DEPOSITION OF GaAs ON $\nabla_X[Si_{1-X}Ge_X]/Si$

A Thomas Swan atmospheric-pressure MOCVD research reactor was used in this work for the growth of GaAs layers on $\nabla_X[Si_{1-x}Ge_x]/Si$ substrates. This system features a horizontal quartz chamber with a water-cooled top-wall, as shown in **Figure 3.6**. Substrates are manually placed onto a graphite susceptor which is then loaded through the rear of the reactor chamber. A quartz-sheathed thermocouple inserted into the radiatively heated susceptor provides feedback to a temperature controller coupled to a water-cooled halogen lamp/reflector heater assembly.

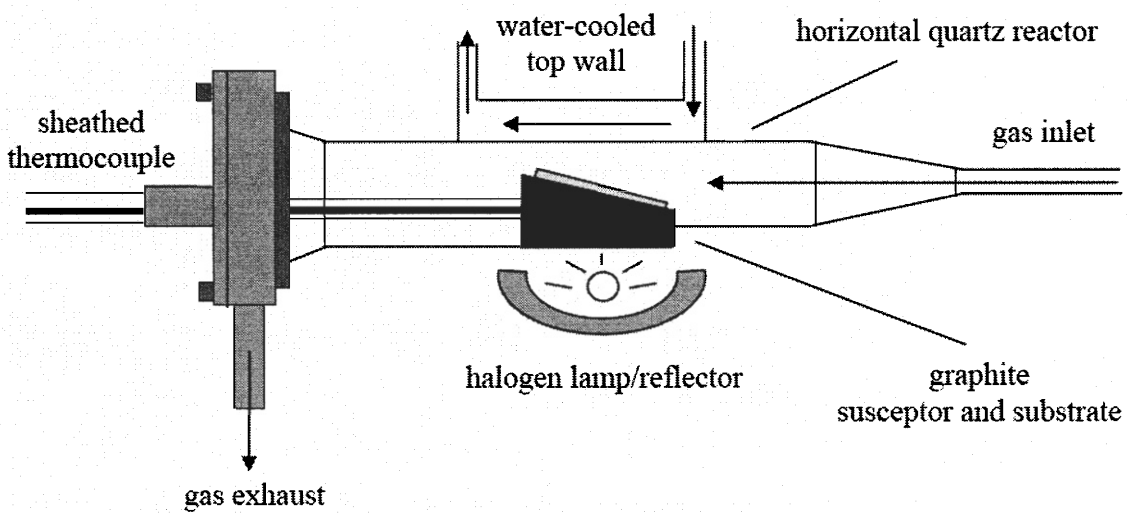


FIGURE 3.6 – Schematic of the MOCVD system used in this work for the growth of GaAs/$\nabla_x[Si_{1-x}Ge_x]$/Si heteroepitaxy. Image courtesy of S. Ting *et al.* (*43-45*)

Substrate material was cleaved from $\nabla_x[Si_{1-x}Ge_x]$/Si wafers to a size of several square centimeters in order to fit the graphite susceptor, which is capable of accommodating up to 50mm diameter wafers. The high-Ge content surfaces were cleaned by alternately dipping in solutions of 30% H_2O_2 and 10:1 diluted HF with de-ionized (DI) water rinses between dips. The final dip in dilute HF left the high-Ge content surface hydrophobic prior to loading into the MOCVD reactor.

A typical GaAs growth cycle started with an initial 10 minute bake at 350 °C and a 5 minute anneal at 700 °C, both in flowing N_2. A ten minute pre-nucleation anneal in flowing N_2 or H_2, with or without flowing arsine (AsH_3), was then conducted at a temperature of 700 °C, and GaAs was subsequently nucleated at the same temperature by adding trimethylgallium (TMG) and AsH_3. The nucleation layer was grown for ~0.1 μm, followed by an additional GaAs growth of varying thicknesses at 700 °C in H_2. At all times, an input V/III ratio >100 was maintained.

3.4 MATERIAL CHARACTERIZATION

A wide variety of techniques were used to characterize the epitaxial films and structures developed. Information on surface morphology, layer thickness, defect density, residual strain, and composition profile were gathered for the various structures used in this work.

3.4.1 TRANSMISSION ELECTRON MICROSCOPY

The internal structure of a semiconductor epilayer, including the quality of the various internal interfaces and the behavior of crystallographic dislocations at these interfaces, can be observed with cross-section transmission electron microscopy (TEM). With properly prepared cross-sections, TEM can provide sub-nanometer resolution capable of accurately measuring thin quantum well structures and distinguishing individual misfit and threading dislocations. The high magnification of modern transmission electron microscopes results in relatively small sampling areas in prepared microscope samples, and thus limits the usefulness of cross-sectional TEM (XTEM) for accurate measurements of semiconductor threading dislocation densities at any levels below 10^8 cm^{-2}. This limit is important to consider when reviewing many of the early reports of reduced threading dislocation densities for integrated GaAs films grown on Si substrates. Accurate dislocation density measurements are only possible with plan view TEM (PVTEM) correlated with defect-selective etching, as will be detailed below. Examples of XTEM and PVTEM micrographs are shown in **Figure 3.7**.

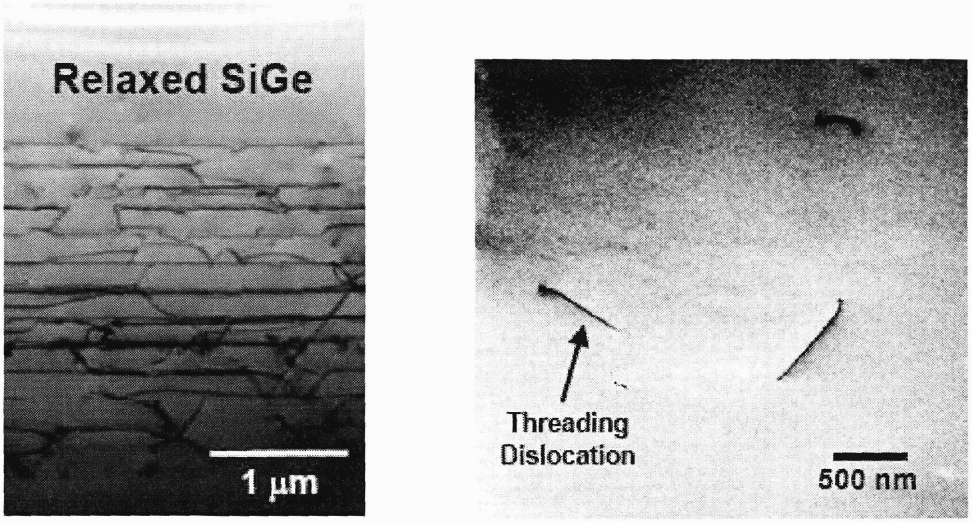


FIGURE 3.7 – (a) XTEM micrograph showing misfit and threading dislocations and (b) PVTEM micrograph showing individual threading dislocations in a relaxed SiGe buffer.

The TEM microscope used for the majority of this work was a JEOL 2000FX operating at 200kV. High-resolution lattice images were taken with a JEOL 2010FX digital microscope capable of 1.2 MX magnification. Microscope samples were prepared by mechanical thinning to less than 50 μm, followed by mounting on a copper handling grid and further polishing to electron transparency (thicknesses of 1 μm or less) using a Gatan precision ion polishing system.

3.4.2 ATOMIC FORCE MICROSCOPY

When the quantification of surface roughness is of importance, atomic force microscopy (AFM) is the optimal characterization technique. A quick surface scan with a stylus allows for accurate determination of surface roughness, as shown in the example in **Figure 3.8**. Built-in analysis tools are employed to determine the root-mean-square (RMS) roughness and the maximum peak-to-valley height. The main drawback associated with this technique is that it samples a very small area of the surface, typically a square

area ranging from about 1x1 μm^2 to 50x50 μm^2. When comparing roughness from different samples, it is advisable to use RMS roughness values determined using similar scan area sizes.

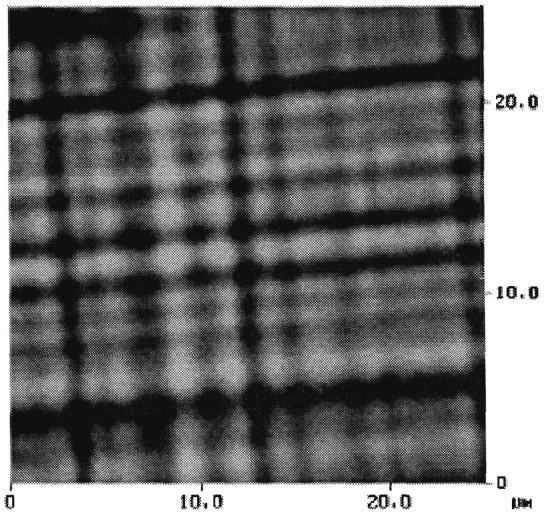


FIGURE 3.8 – AFM surface scan showing the characteristic crosshatch pattern of a SiGe graded buffer.

The AFM system used to characterize the structures grown for work was a Digital Instruments Dimension 3000 Nanoscope IIIa AFM operating in tapping mode.

3.4.3 TRIPLE-AXIS X-RAY DIFFRACTION

X-ray diffraction (XRD) is the most direct and accurate way to characterize the crystallographic quality and residual strain in a deposited semiconductor epilayer. High energy monochromatic x-rays diffracted off the epilayer surface will generate a pattern of diffraction peaks that can be measured and quantified to yield precise information on the symmetry, lattice spacing, orientation, and crystalline quality of the epilayer and substrate crystals. Triple-axis x-ray diffraction, in which the diffracted beam from the sample being measured is passed through an additional analyzer-collimator crystal before being measured, allows for the generation of unique three-dimensional reciprocal space maps

(RSMs) of the diffracted x-ray beams at the sample surface and the precise measurement of residual strain, alloy composition, and crystallographic tilt in the most complex graded buffer structures. In order to attain precise values for composition, strain, and layer tilt, RSMs of both symmetric (e.g. (004)) and antisymmetric (e.g. (224)) reflections are required. An example of a (004) reflection of a SiGe buffer graded to approximately 70% Ge is shown in **Figure 3.9**.

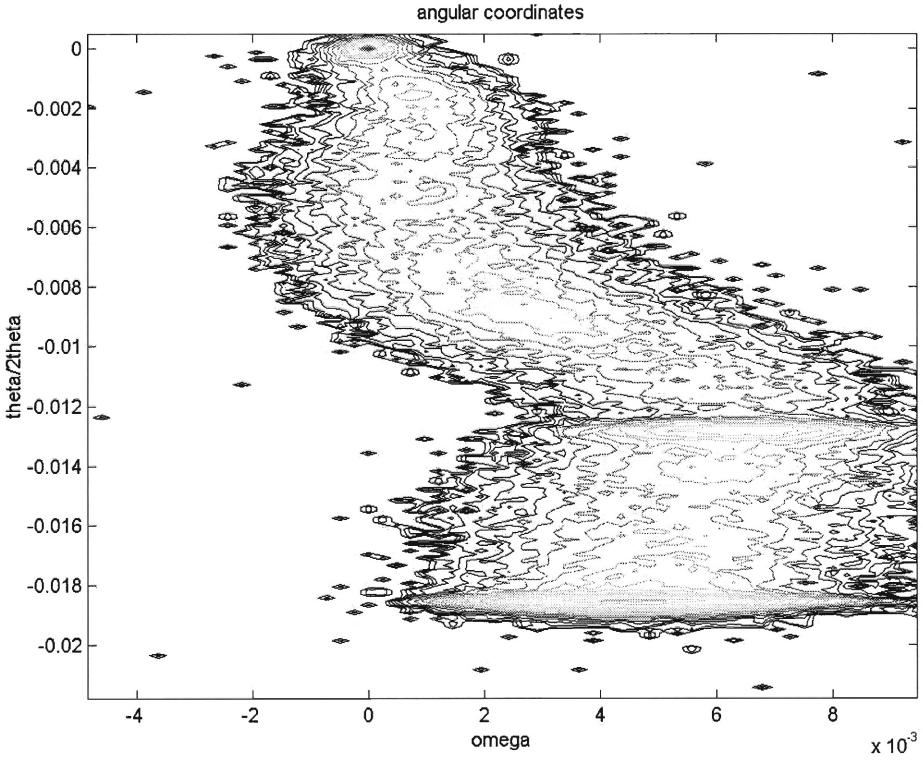


FIGURE 3.9 – Reciprocal space map of the (004) reflection of a $\nabla_x[Si_{1-x}Ge_x]/Si$ structure graded to approximately 70% Ge.

The X-ray diffraction system used to characterize the structures grown for work was a Bede D^3 triple-axis x-ray diffractometer with dual-channel cut Si collimator crystals and a rotating Cu anode x-ray generator operating at 60kV and 200mA.

3.4.4 NOMARSKI CONTRAST MICROSCOPY

Nomarski contrast microscopy, or differential interface contrast (DIC) optical microscopy, can allow sensitive large-scale evaluation of surface microstructure features including crosshatch roughness, dislocation pileups, and surface step bunching. Vertical surface features as small as a few nanometers can be observed at magnifications up to 1000x using DIC methods. A Nomarski image of a strained Si layer on relaxed SiGe buffer is shown in **Figure 3.10**.

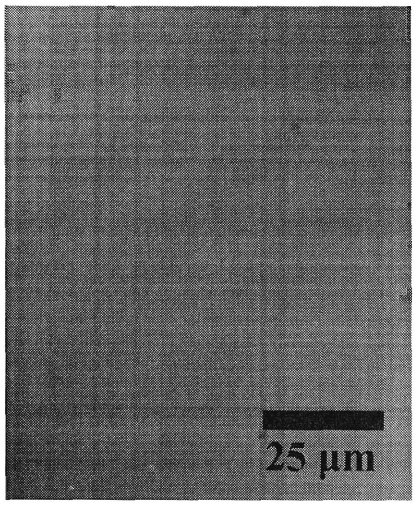


FIGURE 3.10 – Nomarski optical image of a strained-Si layer on a relaxed graded SiGe buffer.

A Zeiss Axioplan optical microscope with a digital camera and differential interference contrast sliders was used for the optical characterization done in this work.

3.4.5 ETCH-PIT DENSITY MEASUREMENTS

A common and dependable method for determining dislocation density in lattice mismatched layers is direct imaging of the defects with plan-view TEM (PVTEM). Unfortunately, the maximum imageable area using electron microscopy is typically smaller than 10 × 10 μm^2. Assuming a magnification of 10,000×, a sample containing 10^5 cm^{-2} threading dislocations will require

hundreds of TEM micrographs to yield a statistically meaningful threading dislocation density (TDD) value. An alternative method for revealing dislocations is selective etching of the sample and subsequent etch-pit density (EPD) measurements. Chemical etching reveals dislocations by selectively attacking their highly strained cores. EPD measurements are suitable for samples containing low ($<10^6$ cm^{-2}) threading dislocations since the etch-pits can be imaged over a large surface area using DIC microscopy, as shown for a Ge virtual substrate in **Figure 3.11**. The diameter of the etch-pit is much larger than the diameter of the corresponding dislocation. Consequently EPD is not applicable to samples containing large defect densities where overlap of the etch pits can underestimate TDD values.

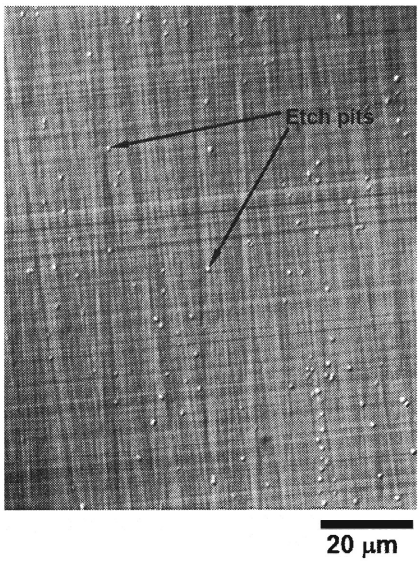


FIGURE 3.11 – Representative image of a Ge/$\nabla_x[Si_{1-x}Ge_x]$/Si sample that was etched with a defect-selective etchant.

Dislocations in $Si_{1-x}Ge_x$ alloys of $x \geq 0.9$ were revealed by etching in a 5:10:11 solution of hydrofluoric acid (HF), nitric acid (HNO_3) and acetic acid (CH_3COOH) with 30 mg of dissolved iodine (I_2). (*46*) This mixture yields an etch rate of ~300 nm/sec, requiring a quick (~1 sec) dip and a high-Ge content SiGe cap thickness of >1 μm to safely prevent etching of dislocations in the underlying

graded buffer. EPD was used in conjunction with PVTEM to monitor the quality of the epitaxial material used in this thesis.

3.4.6 RAMAN SPECTROSCOPY

Peaks of Raman spectra correlate to bond vibrational states. From these peak locations, it is possible to extract information about both SiGe alloy composition and strain in thin films. Raman spectroscopy has the ability to characterize films with film thicknesses as low as 10 nm, with a lateral resolution equivalent to the laser spot size. In contrast, X-ray diffraction typically requires thin films be at least 100 nm thick, and hence is undesirable for the direct analysis of ultra-thin 10 nm strained-Si layers on SiGe.

3.4.7 SECONDARY ION MASS SPECTROSCOPY

Secondary ion mass spectroscopy (SIMS) is a useful technique for determining the composition profile near the surface of a structure. The method utilizes a focused ion beam to sputter ions from the surface of the sample to be probed, and these secondary ions are then collected at a mass spectrometer. These composition data, when combined with the milling rate of the focused on beam for the particular sample, allows for the determination of composition with depth.

SIMS is utilized extensively in **Chapter 7**, where the distribution of implanted H^+ in SiGe alloy layers is studied.

3.4.8 RUTHERFORD BACKSCATTERING SPECTROMETRY

Rutherford backscattering spectrometry (RBS) is a useful technique for measuring the composition profile of a structure. The method employs bombarding a sample with a high-energy He^{+} or He^{++} ion beam. Helium ions which strike the nucleus of the sample being studied will be backscattered into a detector. The energy of these backscattered He ions provides quantitative information about the composition profile of the structure. Additionally, the counts (i.e. number of backscattered ions detected) obtained under a channeling condition, when combined with the counts obtained under a random orientation condition, can allow for the determination of damage with depth.

RBS is utilized in Chapter 7, where the implantation damage in H-implanted SiGe alloy layers is studied. The ion beam used in this work will be a 2.275 MeV He^{++} beam.

3.5 CONCLUSION

An overview was provided of the various growth and characterization methods employed for relaxed graded SiGe buffers, as well as the ε-SiGe and GaAs structures deposited on these buffers. These methods will be applied throughout the remainder of this thesis.

CHAPTER 4: DEVIATIONS FROM IDEAL NUCLEATION-LIMITED RELAXATION IN SiGe/Si

"Egon, this reminds me of the time you tried to drill a hole through your head. Remember that?"

- Dr. Peter Venkman

4.1 INTRODUCTION

Throughout the past three decades there has remained a pervasive interest in the heteroepitaxial growth of lattice-mismatched semiconductor systems, i.e. the growth of films on substrates with dissimilar lattice constants. To date, the relaxed graded buffer approach has remained the state-of-the-art method for monolithically integrating low defect density, lattice-mismatched materials. The method has been successfully demonstrated using several materials systems, including relaxed graded SiGe on Si substrates (i.e. $\nabla_x[Si_{1-x}Ge_x]/Si$) (*8, 9*), InGaP on GaP substrates ($\nabla_y[In_yGa_{1-y}P]/GaP$) (*10*), and InGaAs on GaAs substrates ($\nabla_z[In_zGa_{1-z}As]/GaAs$) (*11, 12*). In particular, the $\nabla_x[Si_{1-x}Ge_x]/Si$ structure has proven successful for the fabrication of high-mobility strained-Si and strained-Ge devices (*16-21*), as well as the $Ge/\nabla_x[Si_{1-x}Ge_x]/Si$ platform for the subsequent growth of III-V devices such as lasers (*22, 23*), waveguides (*24*), and high-efficiency solar cells. (*25, 26*) In this system, scaleable $\nabla_x[Si_{1-x}Ge_x]/Si$ structures with dislocation densities on the order of 10^5–10^6 cm^{-2} can be fabricated across the entire composition range. (*28*)

Previous work on high-quality, low threading dislocation density relaxed graded buffer heterostructures has primarily focused on growth at successively higher temperatures. (*9, 10, 15, 28, 47*) Leitz *et al.* (*28*) explored low-Ge content $\nabla_x[Si_{1-x}Ge_x]/Si$ structures, and found that under nucleation-limited relaxation conditions the threading dislocation density (TDD), ρ, displays the exponential dependence on the growth temperature predicted by Fitzgerald *et al.* (*15*), as given by

$$\rho = \frac{2R_g R_{gr} \exp\left(\frac{E_{glide}}{kT}\right)}{bBY^m \varepsilon_{eff}^m} \qquad [4.1]$$

where R_g and R_{gr} are the growth and compositional grading rates, respectively, m is an exponent with a value generally between 1 and 2, B is a constant, T is the temperature, Y is the modulus, k is Boltzmann's constant, E_{glide} is the activation energy for dislocation glide, and b is the Burger's vector magnitude and the dislocations are assumed to be 60° dislocations. (*15*) Note that this expression is not exact but is an appropriate reduction of the full differential equation required for exact analysis. (*9*) Nonetheless, it is an appropriate guide for thick graded buffers grown at temperatures > 700 °C. The three parameters which offer the most flexibility to the experimentalist are the growth rate, the grading rate, and the growth temperature. It is worth noting, however, that one cannot simply decrease the growth and grading rates to lower the TDD. For example, by grading slower one would produce a thicker buffer, a result which further limits the amount of III-V material that can be subsequently deposited without the appearance of microcracks. (*48*) In addition, by growing slower the growth times could quickly become impractically long. Therefore, the most effective variable is the growth temperature, which should be as high as possible to ensure efficient relaxation with a low threading dislocation density. We also note here that **Eqn. 4.1** represents a steady-state glide model of graded buffer growth. However, we do not track nucleation and annihilation rates in this model as they are in balance, leading to a steady-state expression.

Our previous experiments have persistently demonstrated that the threading dislocation density rises from the mid-10^5 cm^{-2} to low 10^6 cm^{-2} range while grading to a final composition from 50% Ge to a final composition of 100% Ge, as shown in **Figure 4.1**. (*28*) While the development of the TDD in SiGe buffers of $x_{Ge} \leq 0.6$ has been well characterized in the literature, the exact cause of the escalation in the TDD between $0.6 \leq x_{Ge} < 1$ has remained elusive due to less of a concentration on relaxed buffer quality in this composition range. It has recently been demonstrated that approximately 2×10^5 cm^{-2} TDD levels were achieved at Ge compositions as high as $Si_{0.10}Ge_{0.90}$, (*49*) suggesting that the

increase in TDD in high-Ge content SiGe buffers may in fact occur during grading from 90 to 100% Ge.

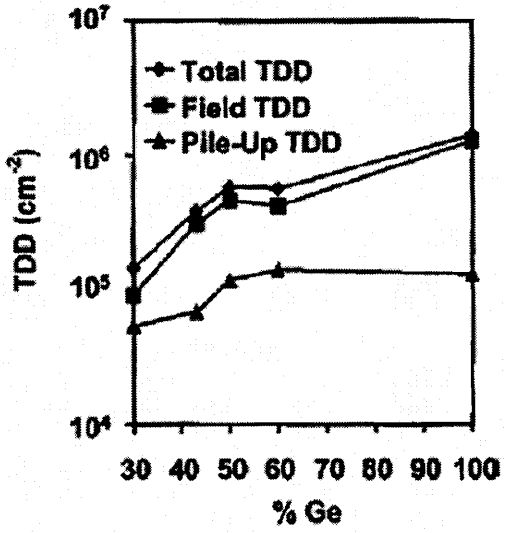


FIGURE 4.1 – Evolution of the TDD in relaxed graded SiGe structures with increasing Ge concentration. Note the dramatic rise observed between Ge fractions of 0.6 and 1. Image courtesy of C. W. Leitz. (*28*)

In this study, we attempt to investigate the rise in dislocation density for Ge-rich buffers and in the process determine the cause of this escalation. Additionally, in accordance with **Eqn. 4.1**, we attempt to offset the detrimental effects of an increased grading rate with a proportionally slower growth rate, thereby potentially maintaining a constant TDD while giving the layers the same amount of time to relax. In this way, the threading dislocation density could theoretically remain constant by allowing dislocations the same amount of time to propagate in order to relax the film, yet one could obtain significantly thinner high Ge-content buffers.

4.2 EXPERIMENTAL OVERVIEW

All growth sets in this study utilized offcut to the nearest {111} from (001) and on-axis 150mm Si(001) substrates, which were cleaned for 10 minutes in a 3:1 H_2SO_4:H_2O_2 solution followed by a 1 minute 10:1 H_2O:HF dip that left the

surfaces hydrophobic prior to growth. The samples were then compositionally graded at 10% Ge μm^{-1} to $Si_{0.50}Ge_{0.50}$ at 25 mT and 900 °C, followed by the deposition of a uniform 2 µm $Si_{0.50}Ge_{0.50}$ cap layer. In order to reduce the crosshatch roughness inherent to such layers and free threading dislocations from dislocation pileups, the samples were then chemical mechanical polished (CMPed) leaving approximately 1.5 µm of $Si_{0.50}Ge_{0.50}$ at the surface. The wafers were again cleaned as described above and growth proceeded to various Ge concentrations between 90 and 100% Ge, at which point each sample was given a 1.5-2 µm cap at the same temperature and pressure as the terminal graded SiGe composition. The experimental parameters of this study are shown in **Figure 4.2** and are modified from previous reports by our group. (*41*) These changes, in accordance with **Eqn. 4.1**, reflected an attempt to maintain the highest possible temperature throughout the 50-100% Ge growth range to allow for improved dislocation kinetics. The upper limit of the growth temperature in the high-Ge content regime was set by the occurrence of gas phase nucleation from the GeH_4 precursor gas used in this study. (*40*) Prior to growth of GaAs, high-Ge content samples were cleaned by alternately dipping in solutions of 30% H_2O_2 and 10:1 H_2O:HF with deionized (DI) water rinses between dips. A final dip in the HF solution left the surfaces hydrophobic prior to growth and GaAs layers were subsequently grown via MOCVD at 700 °C using AsH_3 and trimethyl gallium (TMG) precursors. Details of this III-V growth process on virtual Ge substrates are described elsewhere. (*22*)

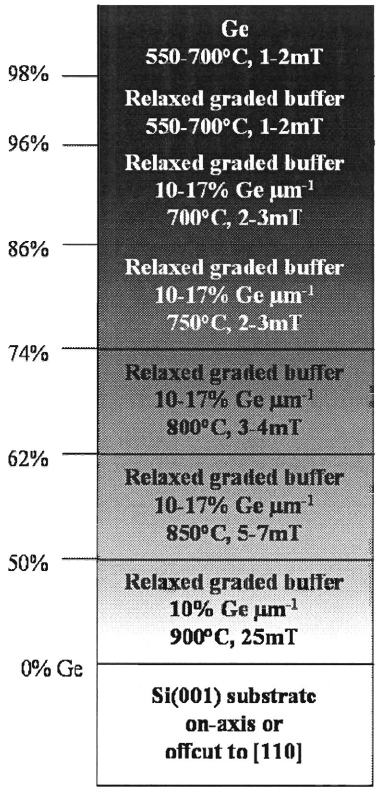


FIGURE 4.2 - Schematic of the structure and growth conditions used for the samples used in this experiment. Shown at left are the Ge concentrations that delineate each growth regime.

Cross-sectional and plan-view transmission electron microscopy (XTEM and PVTEM, respectively), using JEOL 200CX and 2000FX microscopes, were performed in order to the study the microstructure of the heterostructures in this study. Triple-axis x-ray diffraction (TA-XRD), using a Bede D^3 diffractometer with a Rigaku rotating anode source, was used to measure composition and strain. Defect densities of Ge and Ge-rich SiGe layers were measured with PVTEM and etch pit density (EPD), using standard iodine-based etchants (*46*) and a Zeiss Axioplan optical microscope in differential interference contrast (DIC) mode.

4.3 DISLOCATION ESCALATION IN ISOTHERMALLY GROWN RELAXED SiGe BUFFERS

Shown in **Figure 4.3** is a plot of the threading dislocation density as a function of the final Ge concentration in relaxed graded SiGe buffers, all of which were graded at 10 %Ge μm^{-1}.

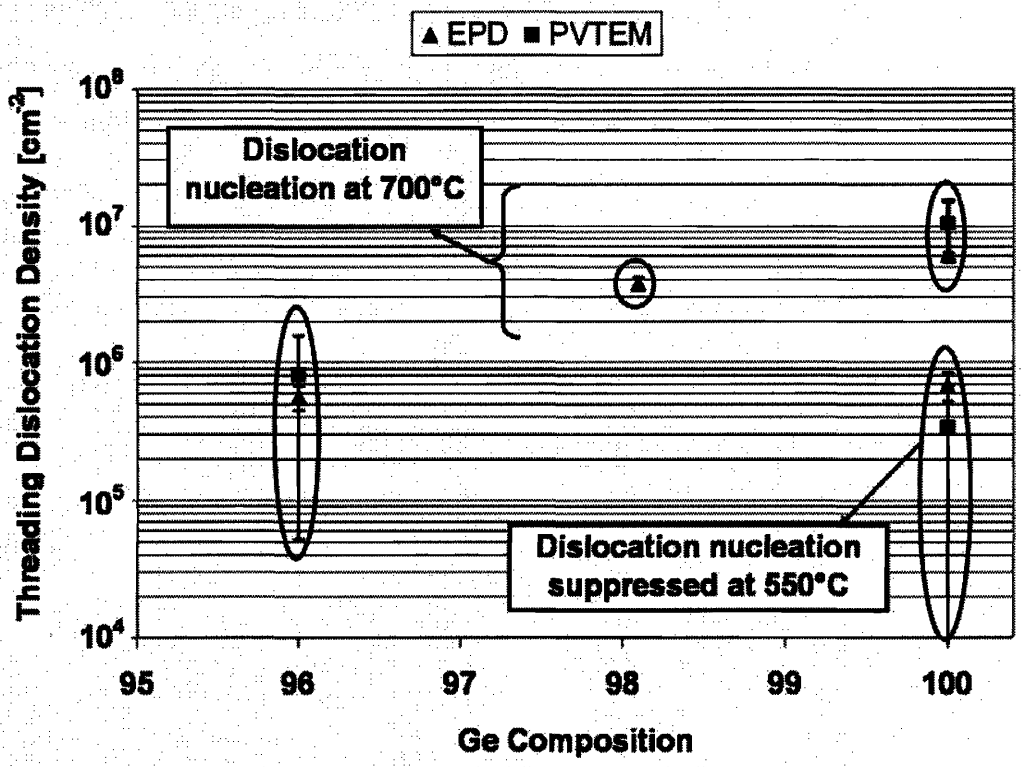


FIGURE 4.3 – Evolution of the TDD with increasing Ge content as determined by various TDD characterization techniques. Error bars reflect 99% confidence intervals.

As can readily be seen in **Figure 4.3**, there is a significant increase in the threading dislocation density at compositions very near to 100% Ge when grown at 700°C. To illustrate, representative PVTEM micrographs and defect-selectively etched Nomarski images comparing samples graded to 96 and 100% Ge at 700 °C on on-axis Si(001) are shown in **Figures 4.4** and **4.5**. These **Figures** clearly demonstrate a lower TDD value for the 96% Ge sample as compared to the 100% Ge sample, rising from approximately 8×10^5 cm^{-2} to 1×10^7 cm^{-2} when graded at 700°C. The escalation of the TDD as pure Ge is reached at 700°C is

striking. In accordance with **Eqn. 4.1**, the increased growth temperatures used in this study should have resulted in more efficient relaxation and a reduced TDD value relative to our previous reports. (*41*) While it has long been observed in our laboratory that the TDD value continually rises with continued grading, this observation has been attributed to a mechanism whereby the combined interference of dislocation pileups and surface roughness during the grading process acts to trap dislocations, necessitating the nucleation of additional threading dislocations to continue relaxing the structure. (*50*) However, such effects are relatively subtle under common growth conditions and therefore the increase of nearly an order of magnitude during grading from 96 to 100% Ge must be attributed to another mechanism upsetting the glide-dominated steady-state expression described by **Eqn. 4.1**.

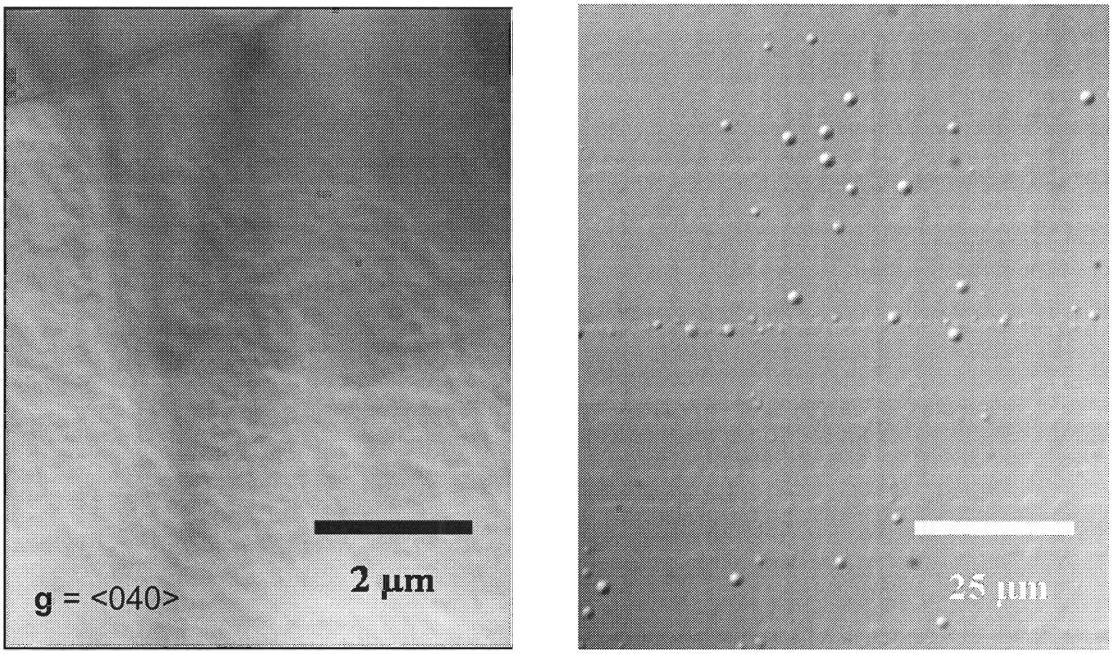
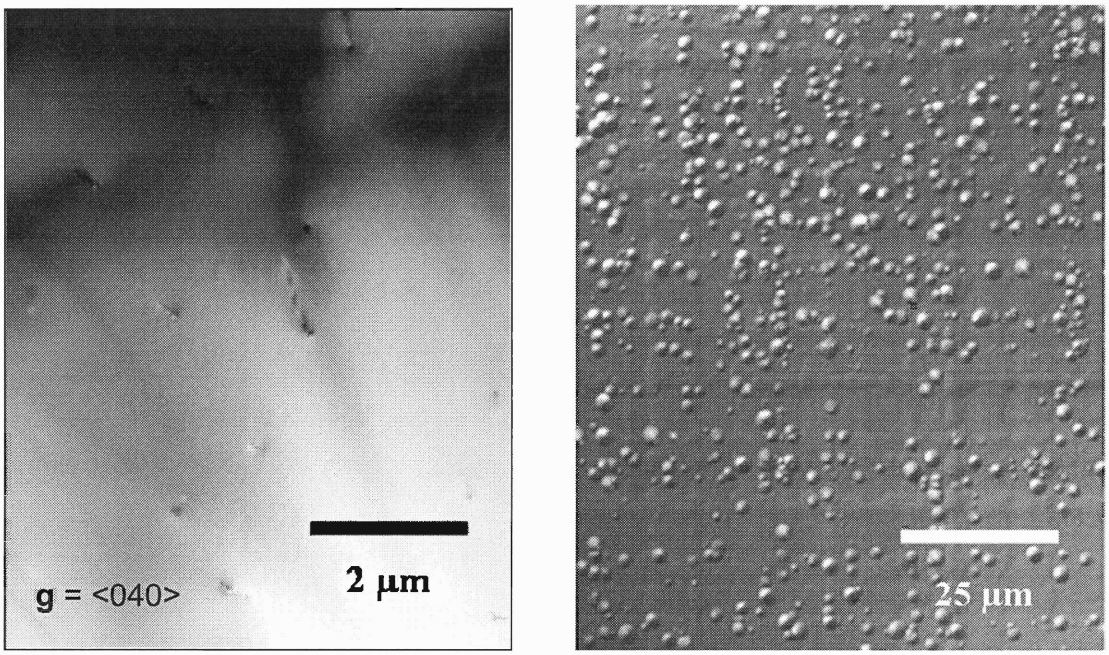


FIGURE 4.4 – Representative (a) PVTEM and (b) defect-selectively etched Nomarski images of a 96% Ge sample grown at 700°C. The average dislocation density for this sample is 8×10^{5} cm^{-2}.



(a) (b)

FIGURE 4.5 – Representative (a) PVTEM and (b) defect-selectively etched Nomarski images of a 100% Ge sample grown at 700°C. The average dislocation density for this sample is approximately 1×10^{7} cm^{-2}.

Previous reports of the dislocation dynamics in bulk SiGe alloys have shown that there is a drastic reduction in yield strength for SiGe compositions approaching pure Ge, which was attributed to a loss of the solid-solution strengthening effect with decreasing Si content. (*51*) Furthermore, as the yield strengths of most crystalline materials decrease with increasing temperature, the higher growth temperatures used in this study for more efficient relaxation relative to previous reports are likely to have exacerbated this effect. Such effects are illustrated in **Figure 4.6**, which shows the dependence of the yield strength of various $Si_{1-x}Ge_x$ alloy compositions. We therefore hypothesize that the 100% Ge cap layer did not relax solely from a nucleation-limited relaxation process; rather, $Si_{0.02}Ge_{0.98}$ and Ge layers are likely much weaker mechanically than even $Si_{0.04}Ge_{0.96}$ at 700°C due to a loss of the solid-solution strengthening effect that a nucleation-dominated (glide-limited) relaxation process results. Such an effect would explain the drastic escalation in TDD value in compositions near pure Ge.

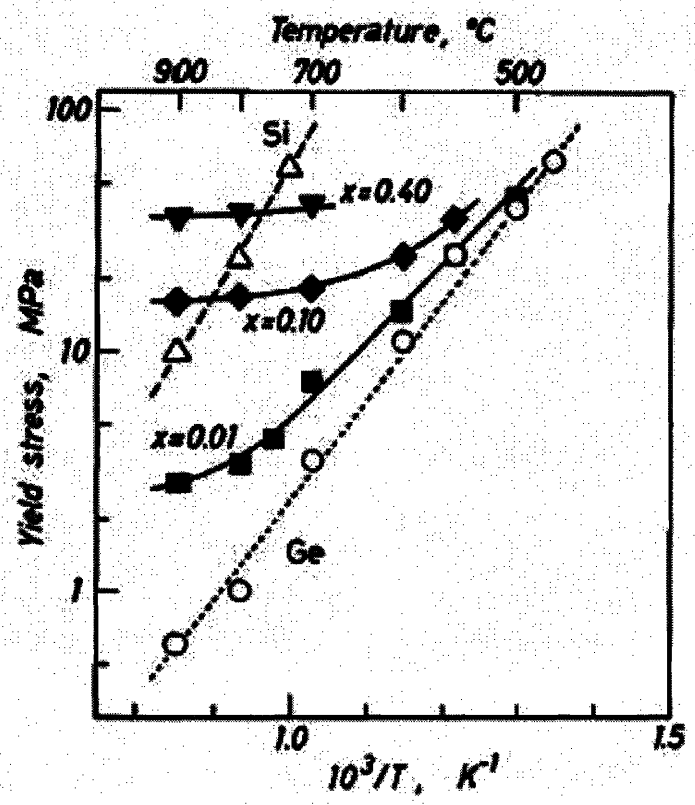


FIGURE 4.6 – Yield strength of various SiGe alloys as a function of temperature. Note that in this Figure *x* refers to the Si content of the layer. The applied strain rate was 1.8×10^{-4} s^{-1}. Image courtesy of I. Yonenaga. (*51*)

To test this hypothesis, virtual Ge on Si structures were grown at a reduced temperature in an attempt to recover sufficient mechanical strength in the $Si_{0.02}Ge_{0.98}$ and Ge layers to suppress the transition to a nucleation-dominated regime. The same procedure described above was followed to 96% Ge, i.e. an attempt was made to ensure the most efficient relaxation possible to 96% Ge by growing at the highest possible growth temperature. The growth temperature was then reduced to 550°C, and a 200nm $Si_{0.02}Ge_{0.98}$ layer and a 1.5 µm Ge layer were deposited. A representative PVTEM micrograph and Nomarski image of this sample after defect-selective etching is shown in **Figure 4.7**. It is important to note that the TDD value for this sample is comparable to that observed at 96% Ge, as shown in **Figure 4.4**. As the grading and growth rates for the 98 and 100% Ge layers were essentially identical at 550°C and

700ºC, this suggests that the reduction in growth temperature for these compositions is directly responsible for arresting the rampant dislocation nucleation in these high-Ge compositions.

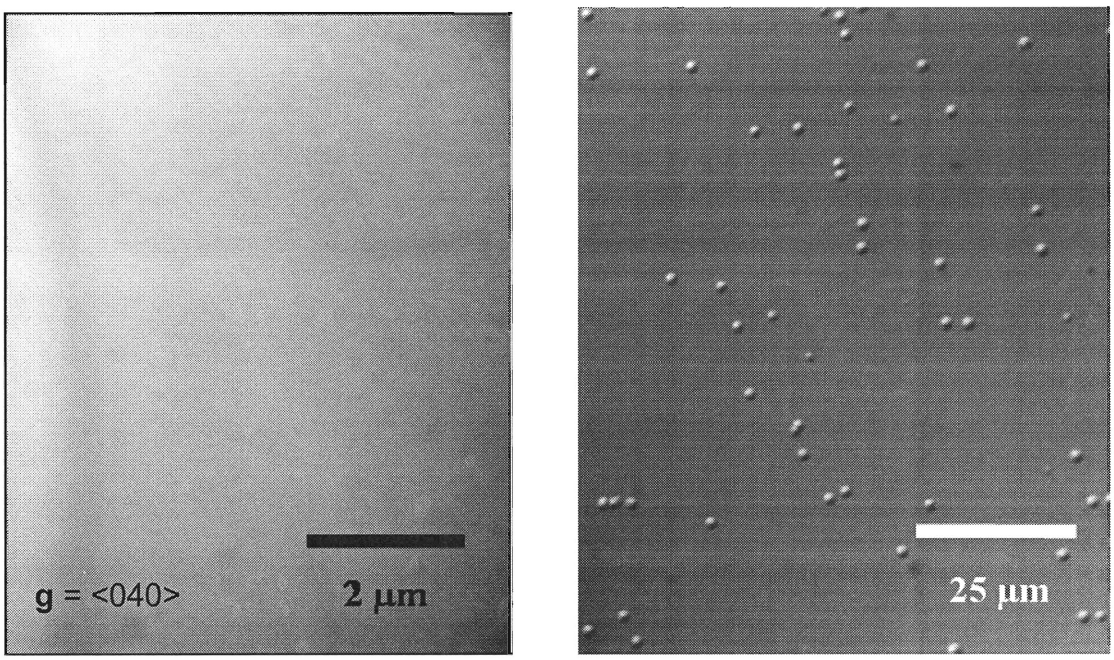


FIGURE 4.7 – Representative (a) PVTEM and (b) defect-selectively etched Nomarski images of a 100% Ge sample grown at 550°C. Note that the EPD value of this sample is essentially identical to that of **Figure 4.4**.

While the reduced growth temperature of 550°C was chosen to explore the possibility of suppressing any mechanical softening of the yield point in these layers, it should be noted that the temperature cannot be significantly reduced beyond this value. Dislocation velocities are known to be exponentially dependent on growth temperature and therefore a severely reduced growth temperature would result in poor dislocation glide efficiency and a concomitant increase in threading dislocation density. Furthermore, as CVD growth depends on the decomposition of source gases, another lower limit is imposed by the fact that growth rates would become impractically low as the growth temperature is reduced below approximately 450°C.

A schematic illustrating the transition from nucleation-limited to glide-limited relaxation is presented in **Figure 4.8**. Thus, while previous work in graded buffers has consistently involved successively higher growth temperatures (*9, 10, 15, 28, 47*), this work demonstrates that the growth temperature can reach a limit where dislocation densities can actually escalate with increasing growth temperature.

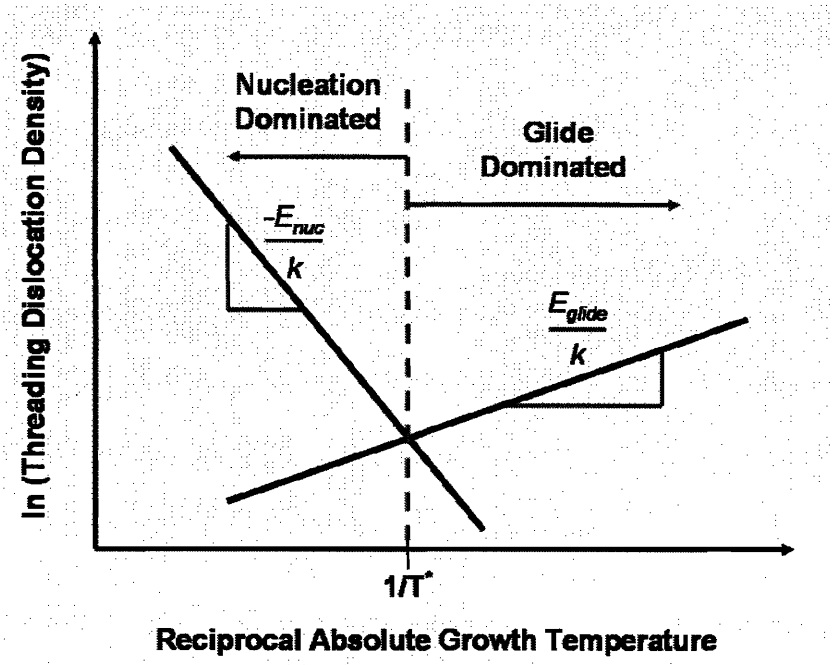


FIGURE 4.8 – Schematic representation of the transition from a nucleation-limited to a glide-limited regime with increasing temperature. Note that the activation energy (magnitude of slope) shown here for nucleation is larger than that of glide, as is generally the case.

Since $Si_{0.04}Ge_{0.96}$ retains a low TDD and GaAs is nearly lattice-matched to this composition at room temperature, it is imperative to investigate GaAs growth on a mixed Si-Ge surface. We deposited GaAs on the $Si_{0.04}Ge_{0.96}$ structure using our previously described MOCVD growth procedure for GaAs on Ge. (*22*) Shown in **Figure 4.9** is a cross-sectional TEM micrograph of a GaAs film grown on a 6° offcut $Si_{0.04}Ge_{0.96}$ sample, which shows that GaAs nucleates on this alloy identically to pure Ge, i.e. without the formation of APBs.

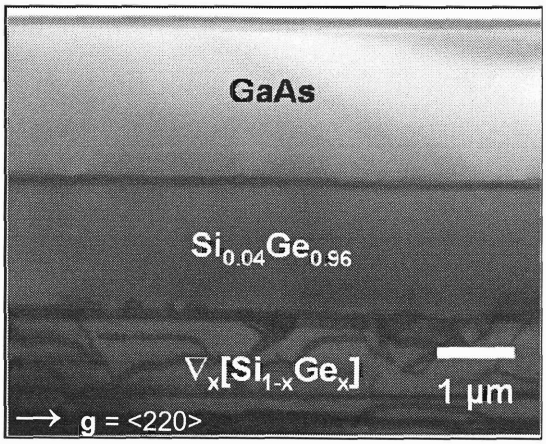


FIGURE 4.9 – XTEM micrograph of GaAs grown via MOCVD at 700°C on $Si_{0.04}Ge_{0.96}/\nabla_x[Si_{1-x}Ge_x]/Si$.

As a result of its close lattice-match with GaAs and the fact that low TDD values are demonstrated without dislocation nucleation or the retention of significant elastic strain, we assert that a composition of $Si_{0.04}Ge_{0.96}$ is an effective way to integrate GaAs on Si with a lower TDD than on 100% Ge buffers.

4.5 ESCALATION IN TDD DUE TO LOCAL REDUCTION IN ε_{eff}

For many III-V devices on Si, such as high-efficiency multi-junction solar cells and vertical-cavity surface-emitting lasers, it would be highly desirable to reduce the thickness of the high-Ge content portion of the SiGe buffer due to the significant thermal mismatch this region adds. To this end, a control set was therefore graded to $Si_{0.04}Ge_{0.96}$ on Si(001) offcut 2° to [110] at various grading rates to observe the effect of increasing the grading rate on the TDD using the optimum growth conditions defined by the previous experimental set.

The effects of altering the growth and grading rates on the threading dislocation density relative to a 10% Ge μm^{-1} control sample are summarized in **Figure 4.10**. Shown in **Figure 4.10** is the TDD value of a sample that was grown at a reduced growth rate, yet for the same amount of time as the 10 %Ge μm^{-1} reference sample. A direct consequence of this approach is that the grading rate

increases proportionally, thereby resulting in a thinner buffer. This sample was grown owing to the fact that it is predicted by **Eqn. 4.1** that one could grade faster, yet grow proportionately slower for the same amount of time and thereby fabricate thinner layers without an increased TDD value. This experiment clearly shows, seemingly in contrast with **Eqn. 4.1**, that such an approach results in a significant penalty with regard to threading dislocation density.

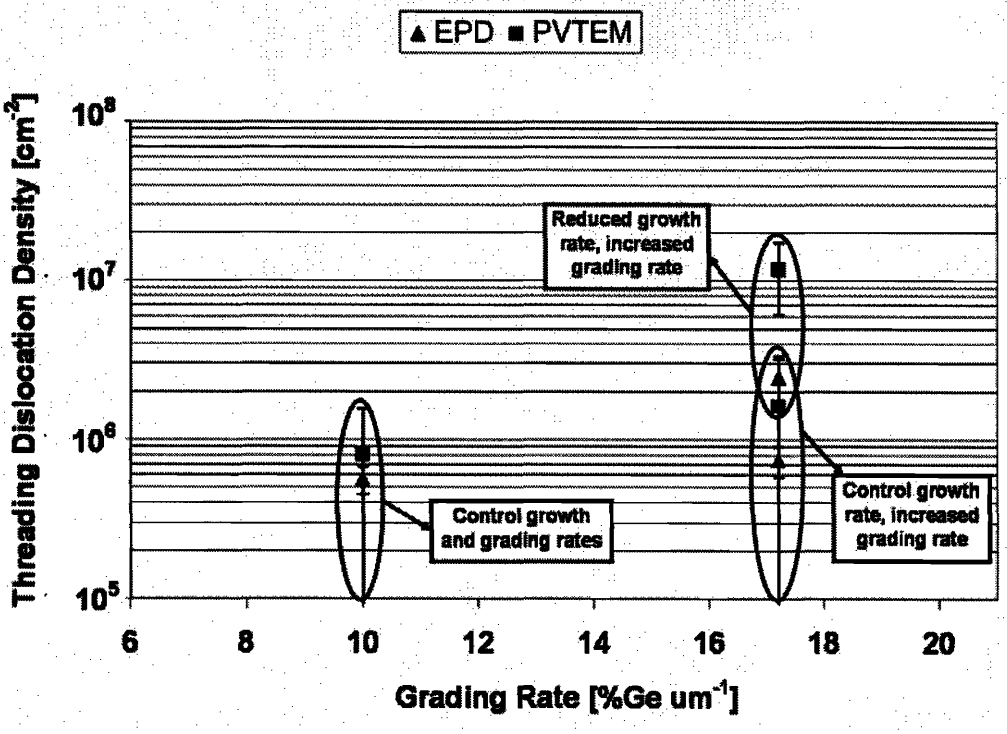


FIGURE 4.10 – Plot of threading dislocation density versus grading rate under various growth conditions as determined by various TDD characterization techniques. Error bars reflect 99% confidence intervals.

Representative PVTEM and defect-selectively etched Nomarski optical micrographs comparing samples graded at 17 %Ge μm^{-1} to 96% Ge at various growth rates are shown in **Figures 4.11** and **4.12**. The growth rate of the sample shown in **Figure 4.11** was roughly half that typically employed for grading to Ge on Si, which is shown in **Figure 4.12**. The strain fields of the misfit dislocation arrays are closer to the surface for these samples than a typical sample graded at 10 %Ge μm^{-1} owing to the higher grading rate, which reduces the critical

thickness, h_c, and brings the misfit dislocations closer to the surface. Therefore, the strain field variation at the surface is larger. In addition, the strain fields influence the surface morphology of the growing layers as adatoms will tend to move from regions of high strain to regions of low strain during growth. (*52*) Thus, when the growth rate is reduced in the presence of these strain fields, adatoms have more time to diffuse on the surface from relatively high to low energy sites. The net result is that the surface evolves to a significantly rougher surface, whereby previously mobile dislocations can subsequently get trapped, thereby resulting in even more strain inhomogeneity in these regions and hence more trapping. The cycle quickly escalates into the observed behavior exhibited in **Figure 4.11**.

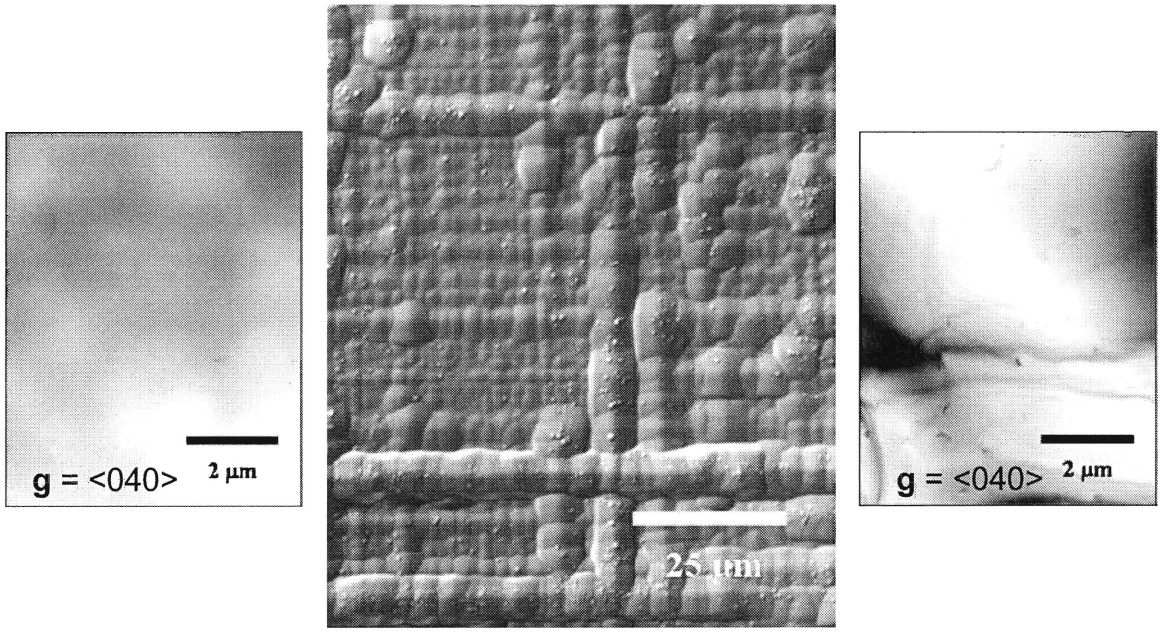


FIGURE 4.11 – Representative (a,c) PVTEM and (b) defect-selectively etched Nomarski images of a $Si_{0.04}Ge_{0.96}$ sample graded at 17% Ge μm^{-1} at a reduced growth rate. The local dislocation density of this sample varies considerably, owing to drastic changes in surface morphology.

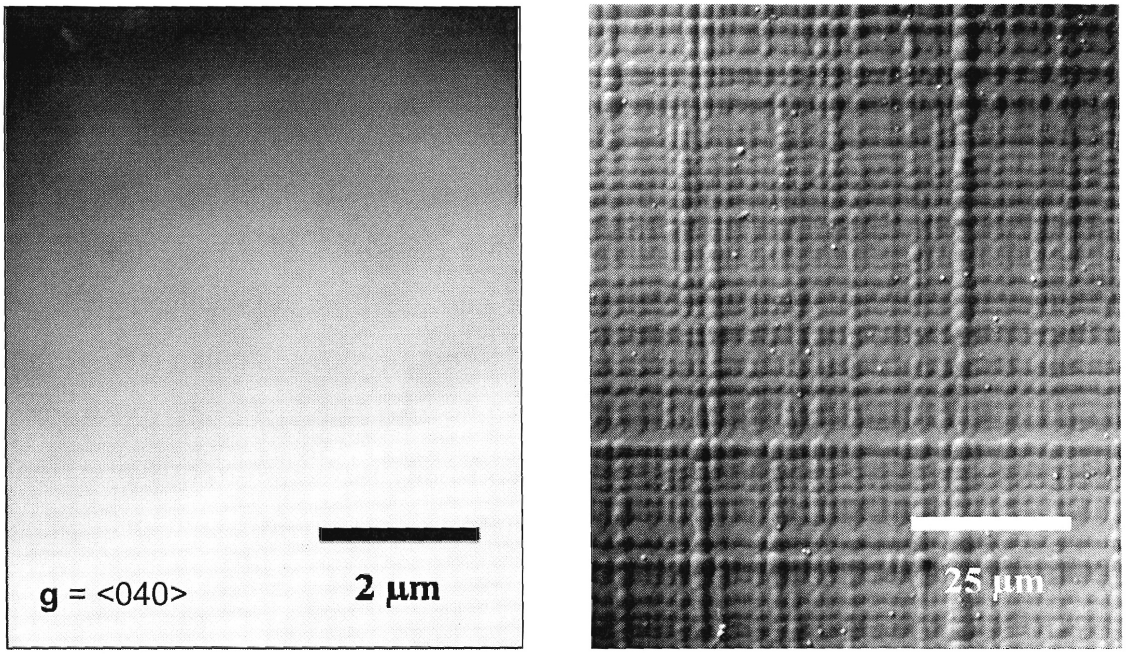


FIGURE 4.12 – Representative (a) PVTEM and (b) defect-selectively etched Nomarski images of a $Si_{0.04}Ge_{0.96}$ sample graded at the same rate as **Figure 4.11** but grown at a higher growth rate. The dislocation density of this sample is approximately 1-2×10^6 cm^{-2}.

The reduction in growth rate relates directly to the observed surface morphology in the following way. The strain fields of misfit dislocations tend to influence the surface morphology of the growing layers, as adatoms will tend to move from regions of high strain to regions of low strain during growth. (*52*) Thus, when the growth rate is reduced in the presence of these strain fields, adatoms have more time to diffuse on the surface from relatively high to low energy sites. The net result is that the surface evolves to a significantly rougher surface, whereby previously mobile dislocations can subsequently get trapped, thereby resulting in even more strain inhomogeneity in these regions and hence more trapping. The cycle quickly escalates into the observed behavior exhibited in **Figure 4.11**.

Implicit assumptions in **Eqn. 4.1** are that the surfaces are planar and that dislocation-dislocation interactions are non-existent. In the faster grading rate, lower growth rate structures the surfaces are not planar and dislocations interact with these surfaces as well as previously-trapped threading dislocations, resulting in dislocation pileups. (*50, 53*) A schematic of such an event is shown below in **Figure 4.13**.

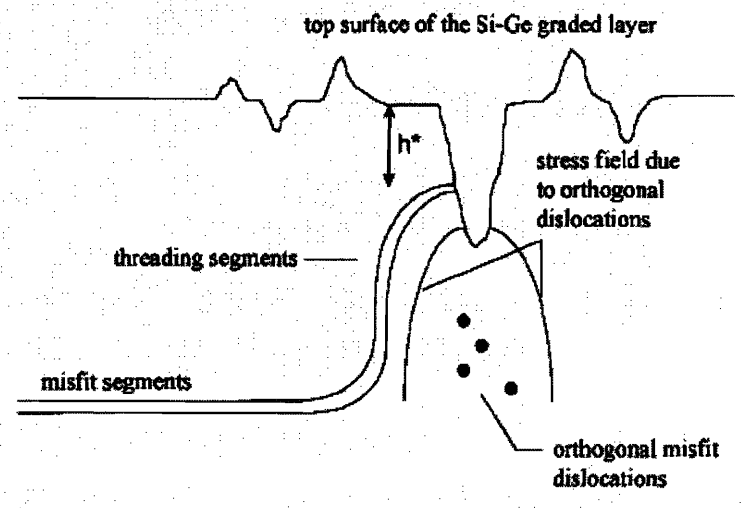


FIGURE 4.13 – Schematic illustrating the mechanism by which threading dislocations may become trapped by orthogonal misfit dislocation segments. Image courtesy of S. Samavedam *et al.* (*50*)

A direct consequence of the formation of dislocation pileups is that mobile dislocations will tend to slow down in their presence, as indicated by the trapping of dislocations exhibited in **Figure 4.11**. Thus, there is a local decrease in the effective elastic strain and a concomitant local decrease in the glide and relaxation efficiencies. As dislocations approach and are trapped in the vicinity of these pileups, it becomes necessary for additional dislocations to nucleate to make up for these deficiencies in the mobile threading dislocation population, in accordance with **Eqn. 4.1**. This results in the formation of the cellular structure shown in **Figure 4.11**, as hypothesized earlier by Leitz *et al.* (*28*), a schematic of which is reproduced in **Figure 4.14**.

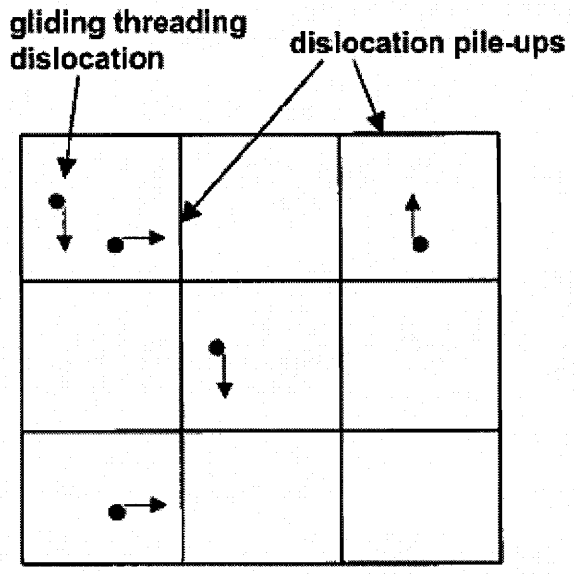


FIGURE 4.14 – Idealized schematic of a predicted cellular dislocation structure. Image courtesy of Leitz *et al.* (*28*)

As illustrated in **Figure 4.14**, dislocations in such a cellular structure would theoretically be able to glide freely within the cells to relieve strain, but would become trapped as dislocation pileups were approached owing to a local reduction in the effective elastic strain. As a result, the mobile dislocation density would soon fall to a level which is insufficient to allow for the continued relief of the applied strain, a condition which would serve to necessitate the nucleation of additional dislocations within the cells. As a result, the density of mobile dislocations would be approximately that required under equilibrium conditions at all times, yet the overall dislocation density could be far greater than that required under ideal relaxation conditions owing to the fact that dislocations would be trapped in dislocation pileups. This is demonstrated in **Figures 4.11** and **4.12**, in which the density of dislocations in the regions without severe crosshatch is approximately equivalent.

It therefore appears that the high overall TDD of this coupled grading-growth rate sample is not due to a breakdown of **Eqn. 4.1**, but essentially due to the fact that the growth rate, R_g, and grading rate, R_{gr}, have strong influences on

the effective strain, ε_{eff}. A rough surface adds barriers to threading dislocation motion through a reduction in ε_{eff} forcing the threading dislocation to glide. In this way, it appears that the presence of an increased grading rate (and therefore increased strain field intensity) and a reduced growth rate allows the surface to evolve closer to its ideal equilibrium crosshatch configuration. Alternatively, it appears that by depositing at high rates, surface diffusion, and hence the formation of an equilibrium crosshatch surface, is suppressed. Thus, we speculate that a suppression of surface roughness through a sufficiently high growth rate may in turn serve to keep ε_{eff} sufficiently high for efficient glide relaxation to take place. Clearly, then, in the "thin buffer regime" R_g and R_{gr} become inherently linked to ε_{eff} through surface roughening, and thus in **Eqn. 4.1**, R_g, R_{gr}, and ε_{eff} are not independent variables.

We note that while we have shown that reduced deposition rates can result in poor quality material, it is likely that deposition rates can be too high for efficient strain relaxation to proceed, as well. This is due to the fact that in the growth of relaxed graded buffers the deposition rate is directly proportional to the rate at which mismatch strain is applied to the system. To illustrate, by depositing too quickly one would likely mirror the results of high-mismatch strain relief, which is well known to result in the rampant nucleation of dislocations.

Thus, we see that for a given growth rate the grading rate cannot be arbitrarily reduced below 10 %Ge μm^{-1} as it would result in an excessively thick buffer. Similarly, for a given grading rate we see that the growth rate cannot be arbitrarily reduced as it allows the surface too much time to evolve towards equilibrium, i.e. a surface with deep crosshatch. However, excessively high growth and grading rates would result in significant dislocation escalation owing to the fact that strain is applied to the system too quickly. Further compounding the problem is that both the grading and growth rates are linked through the effective strain term, ε_{eff} due to surface roughness. While there exists no simple analytic expression linking the grading and growth rates to ε_{eff}, it is clear that in

order to obtain efficient glide relaxation with low TDD values, the growth and grading rates must be judiciously chosen so as to suppress roughening and therefore maintain a moderate global value for ε_{eff}.

4.6 CONCLUSION

We have investigated the evolution of the TDD in relaxed graded SiGe buffers in the high-Ge composition range, using the highest growth temperatures possible without the onset of gas-phase nucleation from the GeH_4 precursor gas used in this study. We found a significant rise in TDD from approximately 8×10^5 cm^{-2} to 1×10^7 cm^{-2} as pure Ge was reached from $Si_{0.04}Ge_{0.96}$ at 700˚C. Similar to previous reports of Ge-rich bulk SiGe alloys, we attribute this observation to mechanical weakening due to a loss of the solid-solution strengthening effect as a pure Ge composition is approached. While this leads to significant dislocation nucleation at the temperatures required for efficient strain relaxation, we demonstrated that this dislocation nucleation in $Si_{0.02}Ge_{0.98}$ and Ge can be suppressed through a sufficiently reduced growth temperature. Thus we have observed a transition from nucleation- to glide-limited relaxation during graded buffer growth.

Furthermore, by coupling the grading and growth rates by growing at reduced growth rates for the same time as a 10 %Ge μm^{-1} reference, we demonstrated a drastic escalation in the threading dislocation density. This is not due to a breakdown of the theoretical basis underpinning **Eqn. 4.1**, but rather the increased roughness induced by the combined effects of more intense strain fields due to higher grading rates and increased surface diffusion. This increased surface roughness leads to a progressive cycle of dislocation trapping and generation, which serves to further reduce the effective strain, ε_{eff}, on dislocations, thereby necessitating an increase in the TDD. In this way, we have shown that the key to obtaining thin, low TDD buffers centers around judiciously choosing grading and growing rates which allow for a high ε_{eff} value to be

maintained, but neither of which is so high that rampant escalations in the dislocation density are observed owing to excessively high strain application rates.

CHAPTER 5: RELAXED SIGE BUFFER BONDING

"Nobody choosed anything!"

– Dr. Peter Venkman

5.1. INTRODUCTION

The relaxed graded buffer approach has defined the state-of-the-art for high quality lattice-mismatched integration for more than a decade. (*9*) However, one significant drawback posed by the method is that several microns of graded material as well as ~1μm or more of uniform composition are typically required to attain essentially relaxed layers of arbitrary lattice constant. The microns of separation between the surface layer and the underlying substrate can significantly complicate certain processes, such as photolithography, thereby limiting the true integration potential of the approach. The method described in this chapter serves to circumvent this problem by transferring the desired surface layer directly to another Si wafer, thereby significantly increasing the integration potential of the relaxed graded buffer method.

5.2 BACKGROUND

The overall process for fabricating engineered substrates via the relaxed buffer bonding method can actually be divided into two distinct sub-processes: wafer bonding and layer transfer. Each of these sub-processes will now be described in detail.

5.2.1 WAFER BONDING

In general, wafer bonding processes involve bringing a first wafer, denoted the donor wafer, in contact with another wafer, which is denoted the handle wafer. The wafers are then annealed for sufficient time at a sufficiently high temperature (time/temperature depending on the materials being bonded) in order to form strong covalent bonds across the bonded interface.

There are several key aspects to successful wafer bonding; particularly important parameters are the state of cleanliness and the surface roughness of

the substrates to be bonded. Particles are another subject of great concern in the wafer bonding process, as a particle will typically serve to disrupt the bonding process over an area much larger than its own size. Essentially, for successful bonding it is desirable to have the cleanest, smoothest wafer surfaces possible prior to bringing the wafers into physical contact. (*54*)

There are two general types of Si-based wafer bonding: hydrophilic and hydrophobic bonding. (*55*) Hydrophilic bonding is typically employed for Si/oxide or oxide/oxide bonding, while hydrophobic bonding is typically employed for direct Si/Si bonding with no oxide layer present at the bond interface. Typical substrate pre-bond clean chemistries for each type are presented in **Table 5.1.**

Table 5.1 – Clean chemistries for hydrophilic and hydrophobic bonding.

Purpose	Hydrophilic [Si/oxide or oxide/oxide]	Hydrophobic [Si/Si]
Organic clean	10 min 3:1 (H_2SO_4:H_2O_2)	10 min 3:1 (H_2SO_4:H_2O_2)
Oxide strip	15 sec 50:1 (H_2O:HF)	15 sec 50:1 (H_2O:HF)
Metal clean	15 min 5:1:1 (H_2O:H_2O_2:HCl)*	15 min 5:1:1 (H_2O:H_2O_2:HCl)*
Oxide strip	N/A	1 min 10:1 (H_2O:HF)

Note that the cleans are similar except that the hydrophilic clean does not employ a final 10:1 H_2O:HF dip, while the hydrophobic clean does (typically without a final DI water rinse). Thus, the hydrophilic cleaning schedule theoretically leaves the bonding surfaces metal-free with a surface chemical oxide terminated by –OH groups, while the hydrophobic cleaning schedule theoretically leaves the bonding surfaces metal-free and H-terminated, similar to the pre-epi clean described in **Chapter 3**. Upon annealing, the general reactions for forming strong, covalent bonds at the interface are given by (*55*)

Hydrophilic bonding: $\text{Si-OH + OH-Si} \rightarrow \text{Si-O-Si + } H_2O_{(g)}$ **[5.1]**

Hydrophobic bonding: $\text{Si-H + H-Si} \rightarrow \text{Si-Si + } H_{2\,(g)}$ **[5.2]**

As shown in **Figure 5.1** for the case of bonding Si substrates, annealing temperatures in excess of 250-300°C and 500-600°C are needed to form strong covalent bonds under hydrophilic and hydrophobic bonding conditions, respectively.

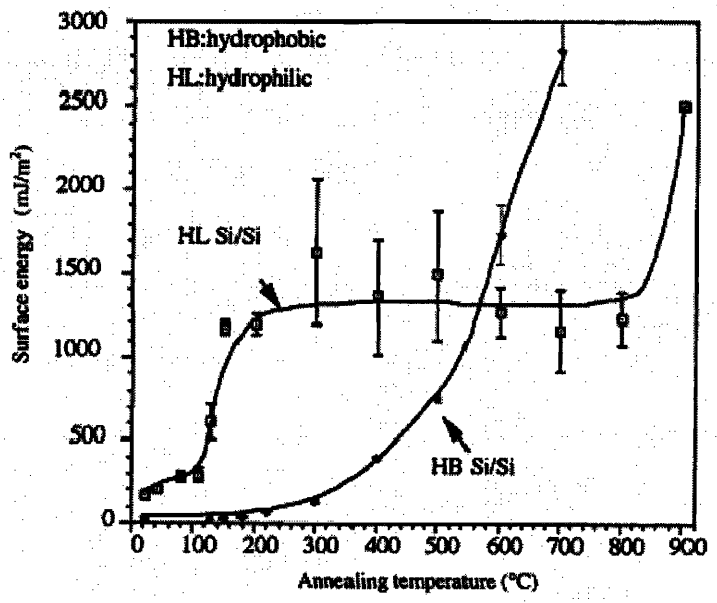


FIGURE 5.1 – Bond strength as a function of anneal temperature for hydrophilic and hydrophobic bonding processes. Image courtesy of Ref. (*55*).

Unfortunately, the high annealing temperatures required for the formation of covalent bonds at the bonding interface can cause severe problems when bonding dissimilar substrates. This is due to the fact that the stress arising from differences in thermal expansion can preclude the possibility for substrates of dissimilar materials remaining bonded after cooldown. Furthermore, while bulk wafer bonding of both GaAs and Ge to Si has been demonstrated, (*56, 57*) GaAs and Ge substrate diameters will always trail that of Si, forever relegating substrates made in this way to trailing-edge CMOS foundries. As a result, it is highly desirable that bonding involve bulk Si wafers for both the handle as well as donor substrates.

5.2.2 GENERAL LAYER SEPARATION TECHNIQUES

After successful bonding, it remains for the desired layer to be physically transferred from the donor wafer to the handle wafer. To this end, two general layer transfer processes are typically employed: the grind and etchback method and the layer exfoliation method.

The grind and etchback process involves bringing the wafers into physical contact and annealing to form covalent bonds, followed by mechanical grinding of the backside of the donor wafer to ~50-100 μm. (*58-60*) Selective chemical etching is then employed to remove the remainder of the donor structure, thereby leaving the intended transfer layer bonded to the handle substrate. (*61-63*) Selective etchstop layers can be employed to provide more control over the etching process.

In the layer exfoliation, or Smart-Cut®, process (*64-66*), molecular or atomic hydrogen ions (H_2^+ and H^+, respectively) are implanted into the donor structure. The inherently low solubility of hydrogen in bulk semiconductors (~10^7 cm^{-3}), (*67*) combined with the damage introduced through the implantation process, results in layer splitting at a depth slightly shallower than the peak implant concentration after annealing the bonded wafer pair for sufficient time/temperature. (*68*) Process flow diagrams of the grind and etchback and layer exfoliation processes are shown in **Figure 5.2**.

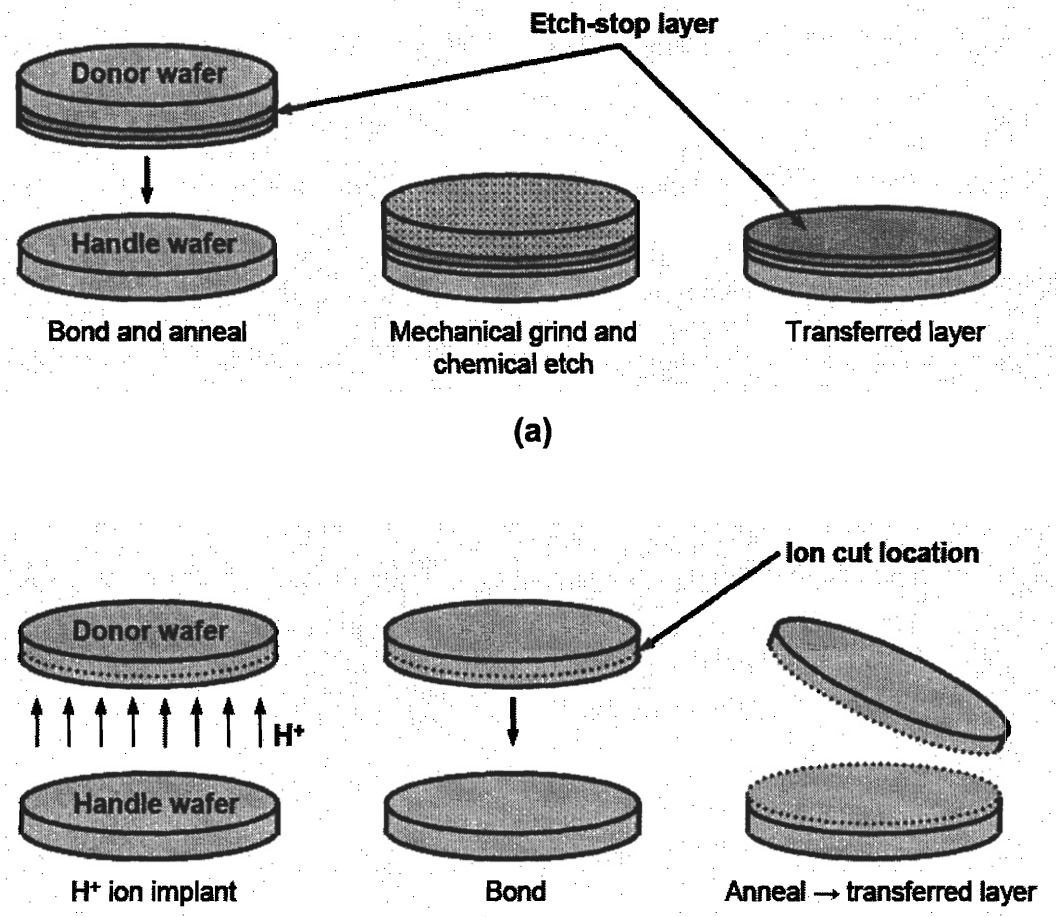


FIGURE 5.2 – Process flow diagrams of (a) the grind and etchback and (b) layer exfoliation by hydrogen-induced splitting processes. Images courtesy of A. J. Pitera. (*13*)

As can be seen from **Figure 5.2**, one significant drawback to the above approaches is that the original donor substrate is essentially discarded after layer transfer is completed. From an economic standpoint, it would be extremely advantageous to recover this investment (especially for donor structures utilizing relatively costly relaxed graded buffers). Accordingly, the topic of potentially reusing $\nabla_x[Si_{1-x}Ge_x]$/Si-based donor structures will be revisited in **Chapter 7**.

5.3 THE RELAXED BUFFER BONDING PROCESS

As discussed in **Chapter 2**, the $\nabla_x[Si_{1-x}Ge_x]/Si$ platform is particularly useful for the fabrication of layers with arbitrary strain states. Relaxed buffer bonding (RBB) is a promising approach wherein a relaxed graded buffer is first utilized to obtain a low dislocation density platform of arbitrary lattice constant. After suitable planarization, a transfer structure is then grown on this graded buffer at a reduced temperature in order to suppress surface roughening, and the donor substrates are subsequently bonded to Si or oxidized Si handle wafers. However, further value is added to the relaxed graded buffer approach in that the RBB method solves several technical issues related to bulk bulking, such as the thermal stress induced from bonding dissimilar substrates. Generalized process flows for adapting the previously mentioned layer transfer processes to the RBB approach are shown in **Figures 5.3** and **5.4**.

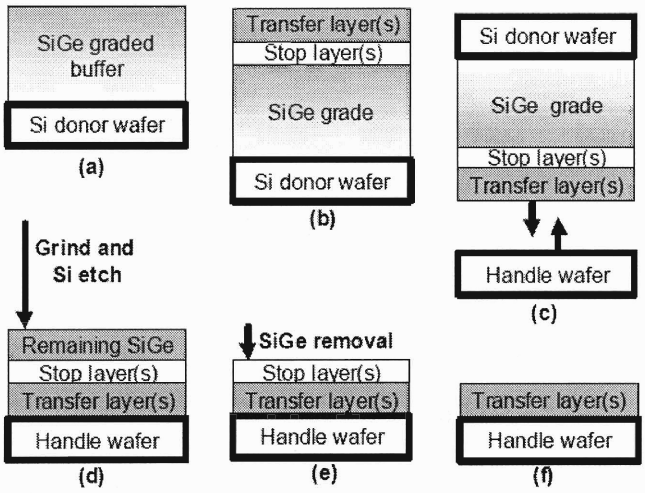


FIGURE 5.3 – Process flow diagram of the grind and etchback using a relaxed graded SiGe buffer, showing (a) growth of SiGe graded buffer and surface planarization, (b) regrowth of etchstop and transfer layers, (c) wafer bonding to handle wafer, (d) backside grinding and Si etch stopping in graded layers, (e) selective SiGe removal, and (f) optional removal of stop layer. Process flow diagram courtesy of G. Taraschi. (*36*)

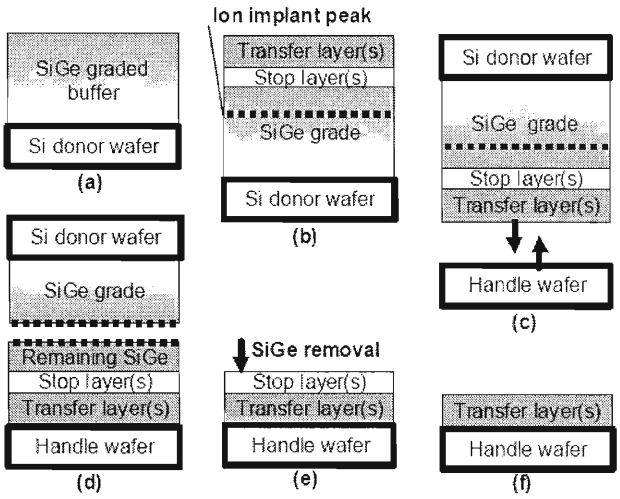


FIGURE 5.4 – Process flow diagram for generic delamination via implantation layer transfer method combined with stop layer(s): (a) growth of SiGe graded buffer and surface planarization, (b) regrowth of stop and transfer layer(s) followed by ion implantation (c) wafer bonding to handle wafer, (d) delamination of the wafer pair at the implant depth, (e) selective SiGe removal stopping on stop layer, and (f) optional removal of stop layer. Process flow diagram courtesy of G. Taraschi. (*36*)

5.4 EXISTING PLATFORMS FROM RELAXED SiGe BUFFER BONDING

The relaxed buffer bonding process outlined above has been employed by our group to fabricate several novel semiconductor heterostructures using SiGe graded buffers. One of the first demonstrations of this technique was silicon-germanium on insulator (SGOI). (*69-71*) A cross-sectional TEM micrograph of such a structure is shown in **Figure 5.5**.

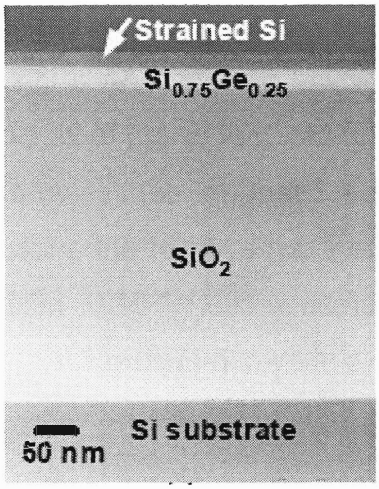


FIGURE 5.5 – Cross-sectional TEM micrograph of SGOI substrate from relaxed SiGe buffer bonding. Image courtesy of G. Taraschi *et al.* (*70*)

Owing to issues related to diffusion and contact metallurgy, the Ge in SGOI leads to the need to re-optimize the CMOS fabrication process. A Ge-free option was soon created to alleviate this problem which incorporates a strained-Si device channel transferred directly to oxide. (*72*) A cross-sectional TEM micrograph of this strained-Si on insulator (SSOI) structure is shown in **Figure 5.6**.

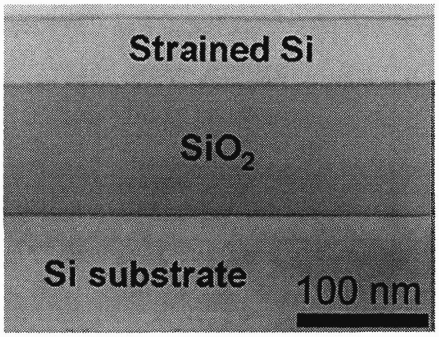


FIGURE 5.6 – Cross-sectional TEM micrograph of SGOI substrate from relaxed SiGe buffer bonding. Image courtesy of T. A. Langdo *et al.* (*72*)

As outlined in **Table 1.1**, the charge carrier mobilities of Ge are far superior to that of bulk Si. Combining the enhanced charge carrier mobilities of

Ge with the added performance of an on-insulator platform would serve to create an enormously powerful CMOS platform. An additional benefit to this Ge-on-insulator (GOI) platform is the fact that owing to its close lattice match, it can also serve as a template for the subsequent deposition of GaAs. Therefore, the GOI structure is promising for the integration of enhanced microelectronic as well as optoelectronic devices. A cross-sectional TEM micrograph of a GOI structure fabricated in our group (*73*) is shown in **Figure 5.7**.

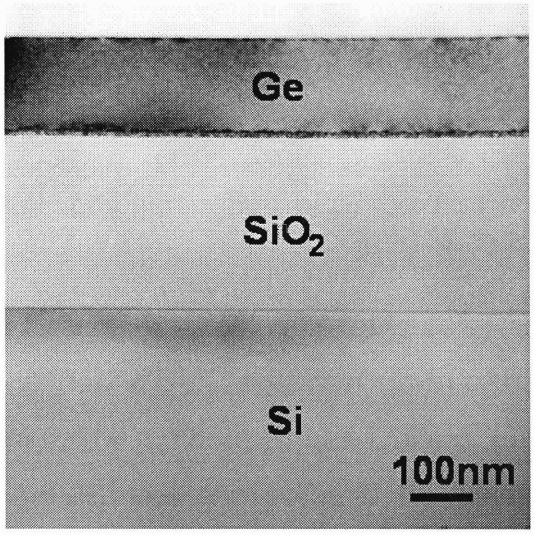


FIGURE 5.7 – Cross-sectional TEM micrograph of GOI substrate from relaxed SiGe buffer bonding. Image courtesy of A. J. Pitera *et al.* (*73*)

5.5 CONCLUSION

Relaxed buffer bonding is a powerful technique for creating and transferring layers of arbitrary strain state to alternate handle wafers. The technique is highly flexible and has enabled the development of a multitude of novel platforms which are attractive for future CMOS generations. The techniques from this chapter will be applied throughout the remainder of this thesis in an attempt to add further value to the relaxed SiGe buffer platform.

CHAPTER 6: NOVEL HIGH THERMAL CONDUCTIVITY CMOS PLATFORMS BY RELAXED SiGe BUFFER BONDING

"Personally, I liked the university. They gave us money and facilities; we didn't have to produce anything! You've never been out of college! You don't know what it's like out there! I've 'worked' in the private sector. They expect 'results'."

– Dr. Ray Stantz

6.1 INTRODUCTION

Over the past decade, the relaxed graded SiGe buffer has enabled the development of a multitude of novel CMOS-compatible strained-Si, -SiGe, and -Ge heterostructure platforms with enhanced carrier transport properties relative to bulk Si. (*8, 9, 16-21, 74*) However, one significant drawback to the relaxed graded SiGe buffer platform is the low thermal conductance offered by the graded structure, which serves to increase the device's operating temperature and therefore reduce the carrier mobilities and drive currents. The research in this chapter is therefore devoted to the study of structures which would retain the increased carrier mobilities of strained-Si devices, yet provide an enhanced thermal conductivity in the vicinity of the device.

6.2 THE SELF-HEATING EFFECT AND THE NEED FOR HIGH THERMAL CONDUCTIVITY PLATFORMS

The Joule heating present in CMOS devices results in a local temperature increase near the device channel, a condition known as the self-heating effect. This self-heating effect is especially pronounced in high power devices and can lead to a significant reduction in both mobility and drain current. (*75*) One way to solve the thermal conductivity issue for high power devices on the relaxed SiGe platform would be to reduce the thickness of the buffer, which is typically on the order of several microns. Previous attempts to realize thin relaxed SiGe layers on Si have included ion implantation of either a Si wafer prior to growth or a strained SiGe layer after growth to drive relaxation. (*76-78*) However, such films are not entirely relaxed and typically have significantly higher defect densities than conventional relaxed SiGe buffer layers. While reports have also been made of SiGe layers grown at significantly reduced temperatures, (*79, 80*) these layers do not approach complete relaxation unless thickness values of at least ~500nm are attained. Furthermore, this low temperature deposition method is incompatible with most commercial growth processes, such as chemical vapor deposition,

which rely on the thermal decomposition of source gases. Clearly, the successful realization of a commercially viable, yet thin and fully relaxed SiGe layer with a low threading dislocation density on Si remains an elusive goal.

An alternative method is to remove the SiGe buffer from the structure altogether while still obtaining the desired properties for the strained film using a layer transfer process. Successful demonstrations of layer transfer using relaxed SiGe buffers have included strained-Si on insulator (SSOI), silicon-germanium on insulator (SGOI), and most recently germanium on insulator (GOI). (*70, 72, 73, 81-84*) For high power devices, however, a significant drawback to the SSOI, SGOI, and GOI platforms is that the intermediate oxide layer results in a dramatically reduced thermal conductivity near the active device regions relative to bulk silicon substrate, similar to the aforementioned strained-Si on relaxed SiGe buffer. Temperatures in SOI devices, for example, have reportedly increased as much as 100 K under static conditions. (*85*)

For high-power applications, it would be most beneficial to couple the performance gain of strained-Si technology with the high thermal conductivity of bulk Si near the active device regions. Strained-Si on silicon (SSOS) substrate technology has recently been demonstrated, (*86*) in which a strained-Si layer is transferred via hydrophobic wafer bonding directly to bulk Si without intermediary oxide or thick (3-5 μm) SiGe layers, thereby making SSOS a direct substitution for silicon substrate. The ability to fabricate such thin, highly strained semiconductor films and place them next to any other semiconductor film creates new directions for engineered substrates. SSOS, for example, is the first homochemical heterojunction, i.e. heterojunction with a significant band offset which is determined solely by the strain state of the materials and not by a composition difference between the layers. Previous reports of similar strained silicon structures grown on relaxed SiGe buffers with similar levels of strain have shown that the strained-Si channel behaves as an electron well with a depth of approximately 130-200 meV. (*87*) The bandgap of such strained-Si layers has

also been determined to be approximately 1 eV. Based on these previous determinations of the band alignment of strained-Si relative to bulk Si, the expected internal band alignment of the SSOS heterostructure is shown in **Figure 6.1**.

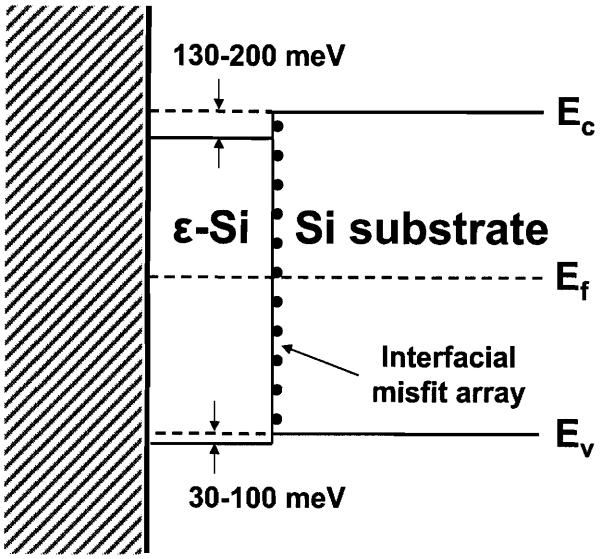


FIGURE 6.1 – Schematic of the expected internal band alignment of the undoped strained-Si (ε-Si) on Si (SSOS) heterostructure. Values shown are for Si under approximately 1% tensile strain. The interfacial misfit array is shown to illustrate its relative location in the structure, not to imply a distribution of levels.

The expected bandstructure of SSOS substrate, coupled to its superior thermal conductivity near the active device region, would seem to make this structure a useful platform for high-power MOS applications. In addition to SSOS substrate, a structure with a thin layer of relaxed SiGe located between a strained-Si layer and bulk Si substrate will be explored. As will be shown, this strained-silicon-on silicon-germanium-on-silicon (SGOS) structure will exhibit greater promise for MOS devices than SSOS.

6.3 FABRICATION AND CHARACTERIZATION OF SSOS AND SGOS

SSOS and SGOS fabrication processes involved growth of relaxed $Si_{1-x}Ge_x$ buffers via ultra-high vacuum chemical vapor deposition (UHVCVD) at 900 °C, which were graded at 10% Ge μm^{-1} to a final composition of approximately $Si_{0.75}Ge_{0.25}$. This composition was selected in order to achieve approximately 1% tensile strain in the subsequent growth of Si channels. The combination of a low grading rate and a high growth temperature results in essentially complete relaxation with a threading dislocation density of approximately 10^5 cm^{-2}. (*28*) The structure was then chemical-mechanical polished (CMP) to reduce the RMS surface roughness to a level suitable for bonding. For SSOS, deposition of 15-18 nm strained-Si transfer layers then occurred at 550 °C in order to preserve planarity at the surface. Similarly, for SGOS, deposition of a strained Si layer with a SiGe spacer and multiple etchstops structure also occurred at 550 °C. A short CMP step was employed after growth of this structure owing to the increased roughness which occurs during substantial regrowth. (*17*) Representative cross-sectional TEM micrographs of such structures are shown in **Figure 6.2**.

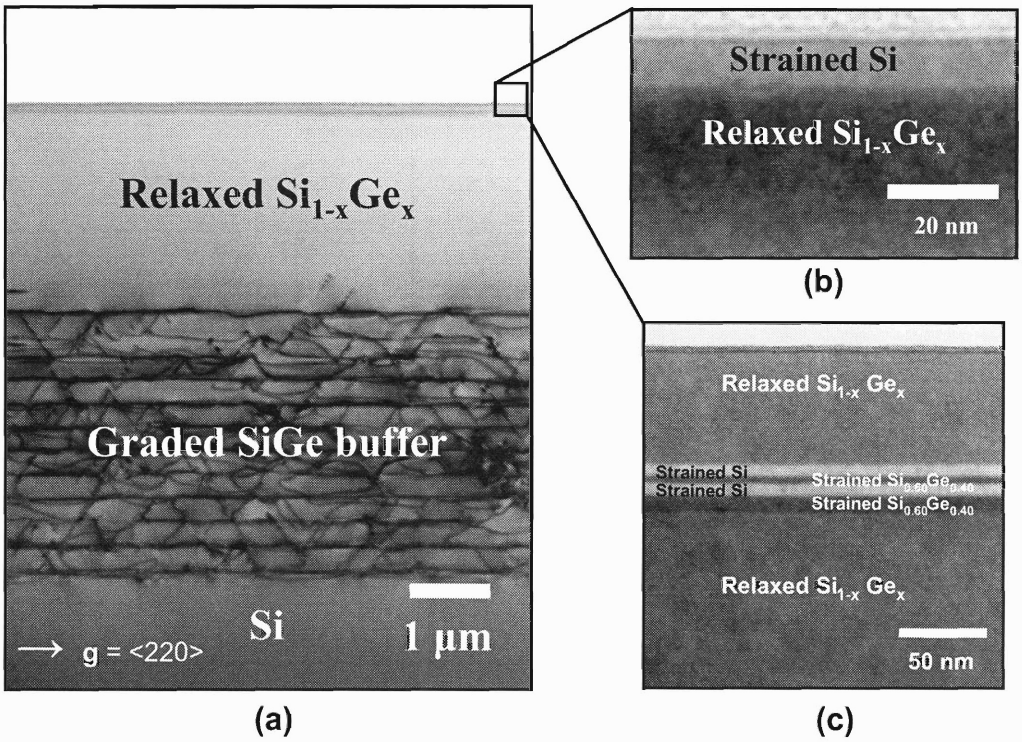


FIGURE 6.2 – XTEM micrographs of (a) a relaxed $Si_{1-x}Ge_x$ (x ~ 0.25) buffer, (b) strained silicon layer on relaxed $Si_{0.75}Ge_{0.25}$ buffer transfer structure for SSOS fabrication, and (c) strained silicon on relaxed $Si_{0.75}Ge_{0.25}$ transfer structure with multiple etchstop structure for SGOS fabrication.

SSOS substrate without intermediate SiGe or SiO_2 layer was fabricated by wafer bonding followed by grind and etch-back, as shown in the process flow diagram in **Figure 6.3**. The strained-Si on SiGe buffer structure and a Si handle wafer were treated with a modified RCA clean consisting of 10 minutes in $3H_2SO_4$:$1H_2O_2$, 15 sec in $50H_2O$:1HF, and 15 min in $6H_2O$:1HCl:$1H_2O_2$ (SC-2) at 80°C. This step left the bonding surfaces hydrophilic, therefore a 1 minute immersion in a $10H_2O$:1HF solution was employed to remove the surface oxide layer and leave the bonding surfaces hydrophobic. The wafer pairs were then bonded at room temperature and subsequently annealed in N_2 at 800 °C for 2 hours to strengthen the bond.

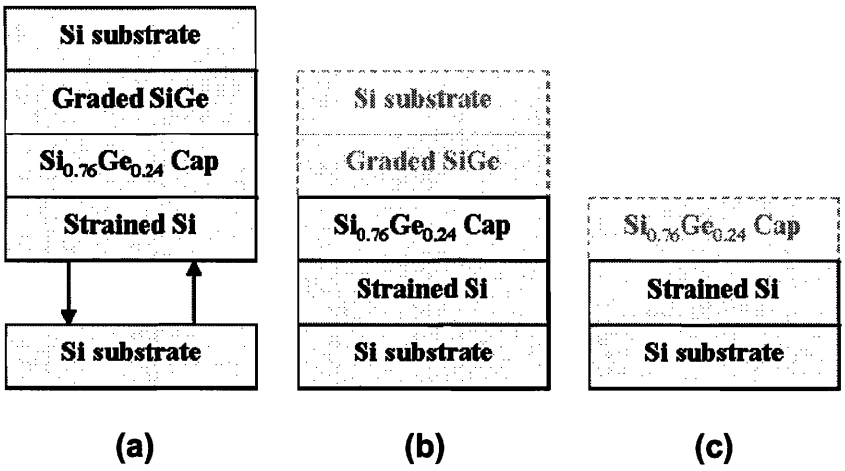


FIGURE 6.3 - SSOS process flow schematic showing (a) wafer bonding, (b) backside removal via mechanical grinding and KOH etching, and (c) final structure after SiGe removal.

Layer transfer was accomplished via mechanical grinding and subsequent etching in a 20 wt% KOH solution to remove the remaining backside of the seed wafer and the low-Ge content portion of the graded buffer. Previous work has shown that the narrowing of the SiGe band gap and the SiGe/electrolyte band alignment leads to a natural etch stop for relaxed $Si_{1-x}Ge_x$ at x~0.20. (*88*) The remaining SiGe buffer was then selectively removed using a dHF:HNO_3:CH_3COOH-based etch, where dHF is a dilute HF solution (100 H_2O:1 HF). Such solutions can have a selectivity of greater than 100 over Si, (*69*) as shown in **Figure 6.4**.

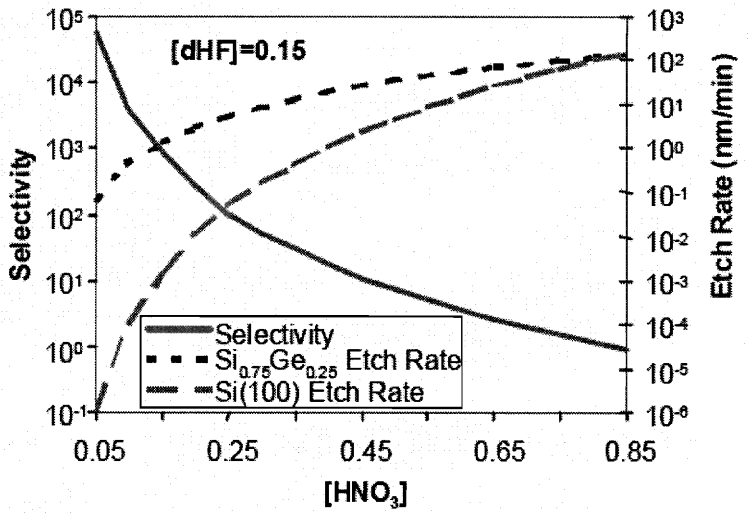


FIGURE 6.4 – Calculated Si and $Si_{0.75}Ge_{0.25}$ etch rates and selectivity for varying [HNO_3] and constant [dHF] = 0.15. Image courtesy of Taraschi. (*36*)

SGOS substrate with a thin intermediate SiGe layer was similarly fabricated by wafer bonding followed by grind and etch-back, as shown in the process flow diagram in **Figure 6.5**.

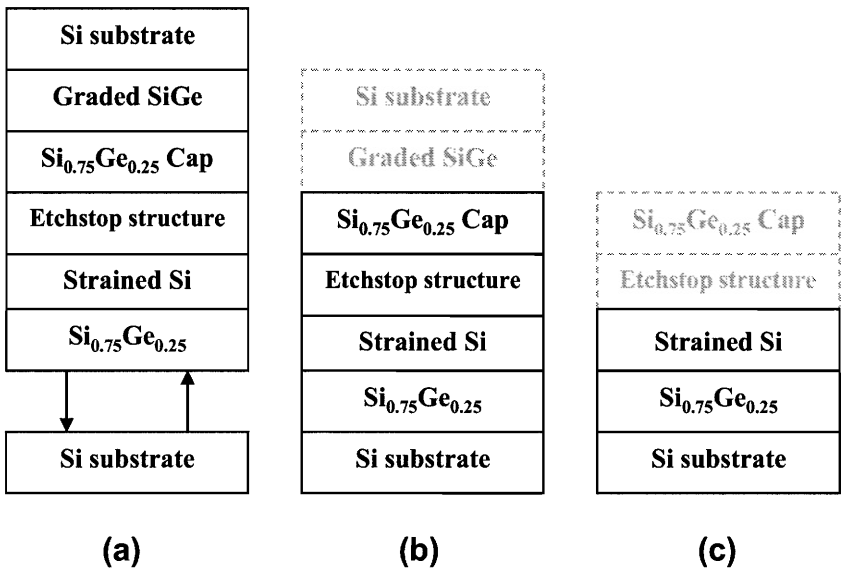


FIGURE 6.5 - SGOS process flow schematic showing (a) wafer bonding and anneal, (b) mechanical grind and KOH etch of substrate and low-Ge content buffer, and (c) final structure after SiGe and multiple etchstop removal.

The fabrication of SGOS was nearly identical to SSOS, except that a multiple etchstop structure was employed to allow for more control of the etching process after transfer. For strained silicon layers and $Si_{1-x}Ge_x$ buffers with x less than ~0.2, a 20 wt% KOH solution was used to remove the remaining backside of the seed wafer and the low-Ge content portion of the graded buffer. For strained SiGe and $Si_{1-x}Ge_x$ buffers with x greater than ~0.2, a dHF:HNO_3:CH_3COOH-based etch was used, similar to the SSOS structure.

6.4 STRAINED SILICON-ON-SILICON (SSOS)

Shown in **Figure 6.6** are cross-sectional transmission micrographs of the SSOS structure (a) before and (b) after SiGe buffer removal. The arrows shown in **Figure 6.6(a)** indicate the location of misfit dislocations with line directions normal to the image plane. Note the average dislocation spacing of these dislocations is approximately 40 nm. The RMS surface roughness of the structure after mechanically grinding and KOH etching was determined via TM-AFM to be approximately 30nm over a 25μm×25μm area, with the crosshatch pattern that is characteristic of relaxed SiGe buffer layers reappearing due to the anisotropic nature of the KOH etch. Shown in **Figure 6.6(b)** is the final SSOS structure, demonstrating the complete removal of the SiGe layer after grinding and etching. At the inset of **Figure 6.6(b)** is a high-resolution TEM micrograph of the bond interface, confirming the absence of an intermediate oxide layer.

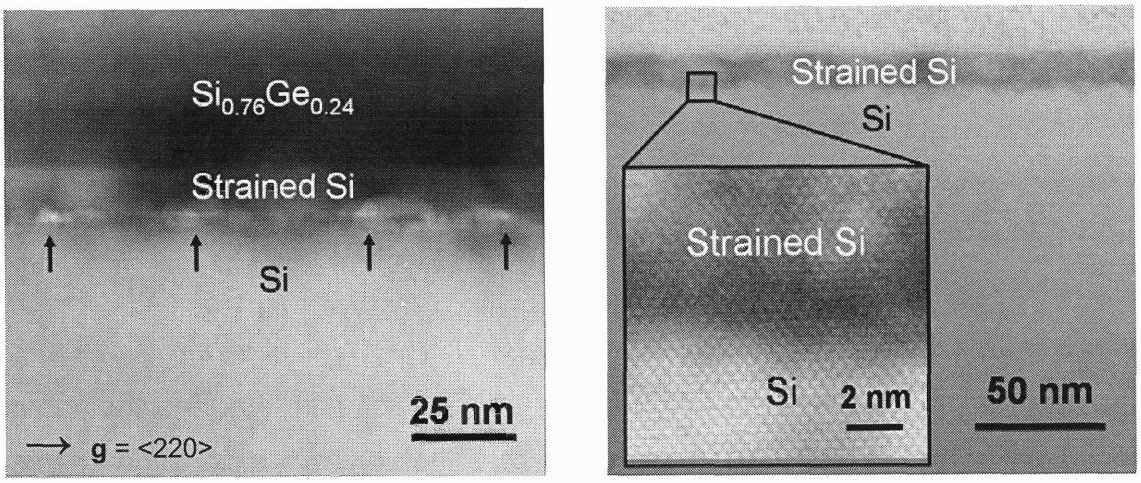


FIGURE 6.6 - Cross-sectional TEM micrographs (a) before and (b) after SiGe layer removal. Arrows in (a) indicate the location of misfit dislocations at the interface.

Shown in **Figure 6.7** is a PVTEM micrograph of the strained-Si/Si interface after SiGe removal. The network of misfit dislocations is formed upon bonding and is *geometrically necessary* due to the differing in-plane lattice constants of strained-Si ($a_{\parallel}$ = 0.548nm for strained-Si on $Si_{0.76}Ge_{0.24}$) and bulk Si ($a_{\parallel}$ = 0.543 nm). The lack of a perfectly orthogonal array is due to the difference in miscut between the wafers.

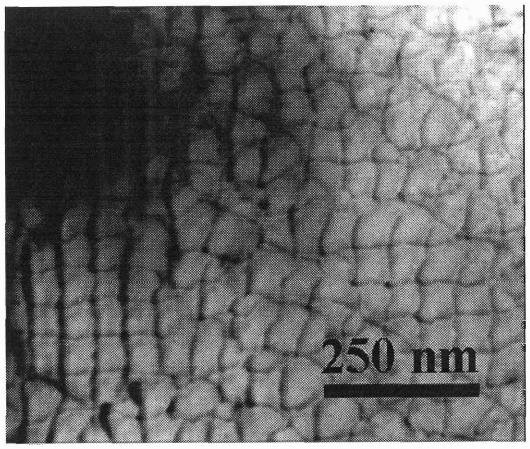


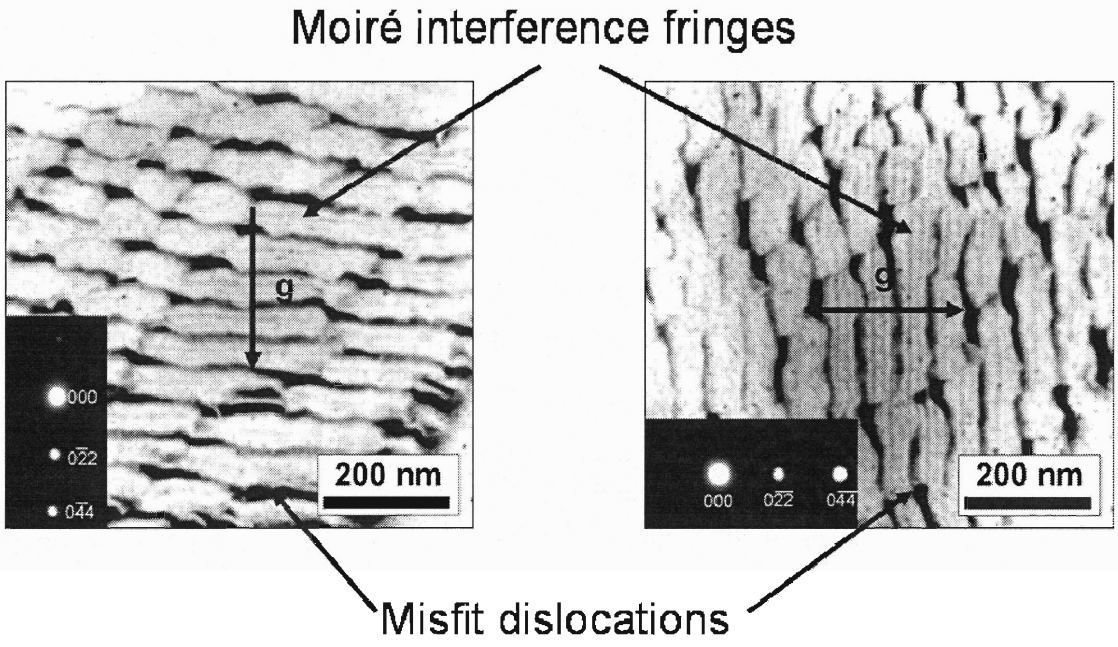
FIGURE 6.7 - Plan-view TEM micrograph showing the misfit array at the bonded strained-Si/Si interface.

If we assume no slight miscut or rotation, we would expect a misfit dislocation spacing, *S*, of

$$S = b_{eff}/\delta = b/(\Delta a/a_{Si}) \qquad [6.1]$$

where b_{eff}, is the effective Burgers vector, δ is the level of strain (0.0094 for strained Si on $Si_{0.76}Ge_{0.24}$), and Δa is the difference in the in-plane lattice constants of the layers. Substitution of these values gives a dislocation spacing of 40.9nm, which is approximately the observed spacing. The effective Burgers vector, b_{eff}, is equal to $\mathbf{b}_{eff}$=a/2[110] if the interfacial dislocations are edge in character. Edge character of these interfacial dislocations is to be expected, as the misfit array is formed by bonding and not by individual dislocation glide. The interface array is not formed by dislocation glide and therefore the quality of the strained Si layer is determined by the original threading dislocation density in the relaxed buffer and is unrelated to the interface array. Furthermore, in strained Si/SiGe material, the strain is retained if the strained silicon layer thickness is below the critical thickness, leaving Ge interdiffusion as the only mechanism which can relieve strain. (*74*) Based on these previous results, the thermal stability of subcritical thickness SSOS substrate is expected to be well within the thermal budget of leading-edge CMOS fabrication.

While **Figure 6.7** confirms that an orthogonal dislocation array exists at the interface in SSOS, it remains to be shown that the dislocation array is in fact edge-type in nature. PVTEM micrographs of the strained Si/Si interface are presented in **Figure 6.8** under various 2-beam conditions.



(a) (b)

FIGURE 6.8 – A series of plan view TEM micrographs of the strained Si/Si interface, taken using different g directions for Burgers vector analysis of the dislocation network: (a) g=0-44 and (b) g=0-4-4 conditions.

As seen in **Figure 6.8**, there is a periodic array of Moiré interference fringes that is always perpendicular to **g**, with a periodicity of approximately 10 nm. The equation for relating the spacing, S_M, of Moiré interference fringes to the lattice mismatch between two layers is:

$$S_M = \frac{d_{\varepsilon\text{-Si}} d_{\text{Si}}}{d_{\varepsilon\text{-Si}} - d_{\text{Si}}} = \frac{d_{\varepsilon\text{-Si}}}{\delta} \qquad [6.2]$$

where $d_{\varepsilon\text{-Si}}$ and d_{Si} are the interplanar spacing of the strained-Si and Si layers (approximately 0.097nm and 0.096 nm respectively under **g** = 440-type conditions) and δ is the lattice-mismatch between the two layers (0.0094 for the case of strained-Si from relaxed $Si_{0.76}Ge_{0.24}$). (*89*) Substitution of the values results in a calculated Moiré fringe spacing of 10.3 nm, consistent with that shown in **Figure 6.8**.

Given that the transferred strained-Si layer should have the same *in-plane* lattice constant as the $Si_{0.76}Ge_{0.24}$ layer from which it was transferred (0.548 nm), one can calculate the expected misfit dislocation spacing at the interface for a given twist misorientation, θ. A more detailed analysis of the expected dislocation spacing, S_D, is related to the in-plane lattice constants of the bonded layers and the twist misorientation angle θ by

$$S_D = \frac{a_{\varepsilon\text{-Si}} a_{Si}}{[2(a^2_{\varepsilon\text{-Si}} + a^2_{Si} - 2\, a_{\varepsilon\text{-Si}} a_{Si} \cos\theta)]^{1/2}} \qquad \textbf{[6.3]}$$

where $a_{\varepsilon\text{-Si}}$ and a_{Si} are the interplanar spacing of the strained-Si and Si layers (0.548 nm and 0.543 nm, respectively) and θ is the in-plane misorientation angle between the transferred layer and the Si handle wafer. (*90*) The twist angle between the layers, θ, was found via asymmetric {224} triple-axis x-ray diffraction to be approximately 0.25°. (*91*) Substituting the values of the in-plane lattice constants of the bonded layers and the twist angle of 0.25° into **Eqn. 5.3** results in a calculated dislocation spacing of 38 nm, in excellent agreement with the spacing of the [110]-type dislocation array exhibited in **Figures 6.7** and **6.8**.

We note that while we have achieved the fabrication of SSOS, complete layer transfer was not accomplished, partially owing to non-uniform etching of dislocation cores during the SiGe removal process. Shown in **Figure 6.9** is a cross-sectional TEM micrograph of such an event. Evidence that the selective etching seen in **Figure 6.9** is due to the preferential etching of dislocation cores is offered by the fact that the interspacing of the etched regions is identical to that of the dislocation spacing seen in **Figures 6.6** and **6.7**.

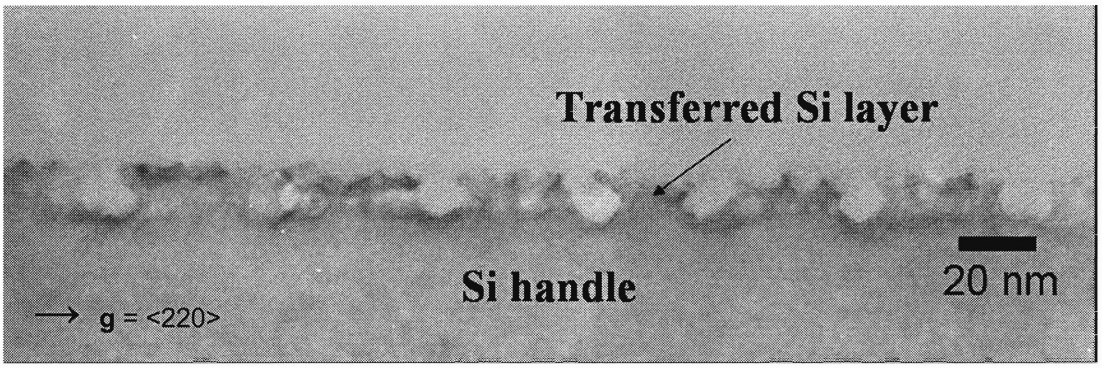


FIGURE 6.9 - Cross-sectional TEM micrograph showing preferential etching of the misfit array at the bonded strained-Si/Si interface.

A further cause of concern for SSOS substrate is that recent work has shown that misfit dislocations at the interface of strained silicon layers on relaxed SiGe buffers can create large off-state leakage currents in MOS devices. (*92*) Misfit dislocations are responsible for decreasing the local gate length, thus worsening short channel effects. The gate length shortens by source and drain dopants rapidly diffusing along misfit dislocations. The interfacial misfit array in SSOS differs greatly from the typical interface dislocations at the strained Si/SiGe interface. The strained Si/SiGe interface dislocations are typically very straight and are also at a much greater spacing than the SSOS dislocations. As such, due to differences in dislocation structure between the strained Si/SiGe and SSOS platforms, further study is needed to judge the electrical impact of dislocations in SSOS CMOS applications.

Source-drain contacts typically penetrate deeper into the substrate than the critical thickness of strained Si on relaxed $Si_{1-x}Ge_x$ (h_c typically ~10-15nm for x~0.2-0.25), making overlap of the source-drain regions and the interfacial misfit array unavoidable. A schematic of such a situation is shown in **Figure 6.10**.

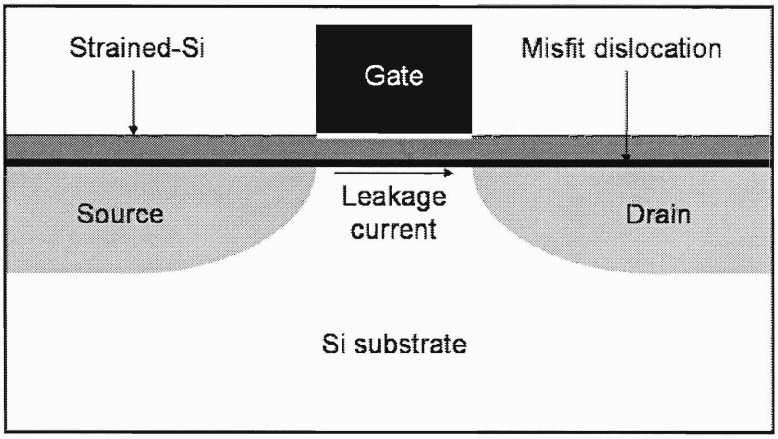


FIGURE 6.10 – Schematic diagram showing the overlap of source-drain contacts with the interfacial misfit dislocation array in SSOS substrate.

Simply increasing the thickness of the strained Si layer is not possible, as critical thickness concerns essentially preclude this possibility. SGOS would solve this expected problem by physically distancing the source-drain contacts from the misfit dislocation array, as shown in **Figure 6.11**.

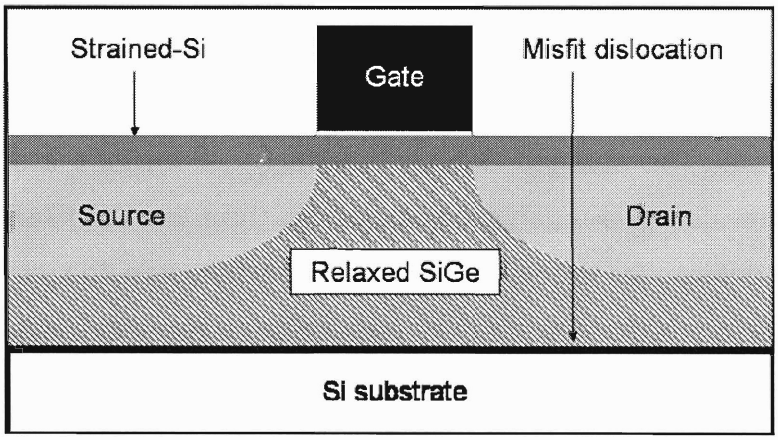
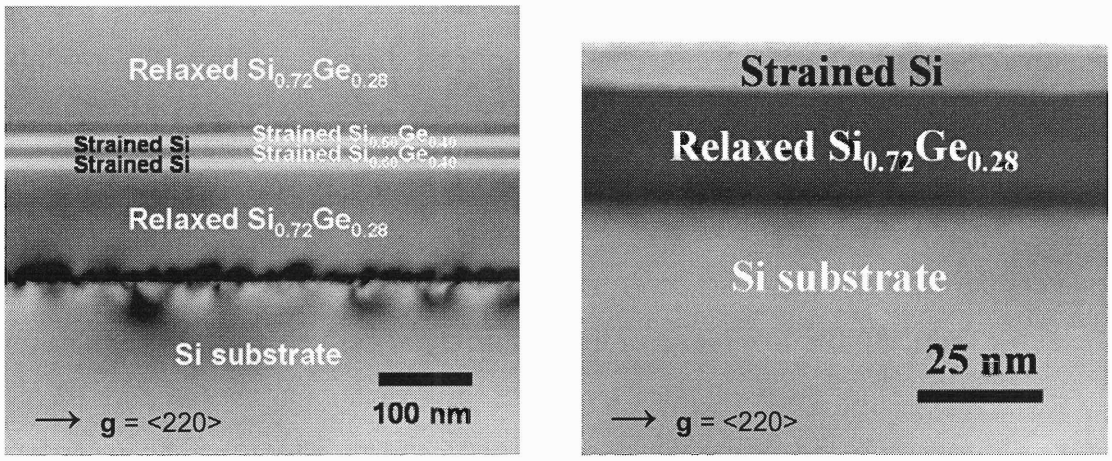


FIGURE 6.11 – Schematic diagram showing the lack of overlap between the source-drain contacts and the interfacial misfit dislocation array in SGOS substrate.

As a result of the elimination of the overlap of the source-drain regions with the misfit dislocation array, SGOS is expected to be a superior MOS device platform as compared to SSOS.

6.5 SILICON GERMANIUM-ON-SILICON (SGOS)

Shown in **Figure 6.12** are XTEM micrographs of the SGOS structure (a) before and (b) after SiGe buffer removal. As shown in **Figure 6.12(b)**, a thin layer of SiGe separates the strained-Si surface channel from the bulk Si substrate. The inclusion of this thin SiGe spacer layer is expected to aid fabrication and device performance in two key ways. First, since the SiGe distances the surface strained Si layer from the interfacial array, it is expected that the preferential etching issues exhibited in **Figure 6.8** should be greatly reduced. This is primarily due to the fact that the strain fields of edge dislocations have a r^{-1} dependence, where r is the distance from the dislocation core. Thus, by inserting a layer of relaxed SiGe, the effect of the strain fields on the etching properties will be reduced. Additionally, the inclusion of the relaxed SiGe layer also serves to eliminate the overlap of MOSFET source-drain contacts with the interfacial misfit array when the thickness of the SiGe layer is greater than typical source drain junction depths. This would eliminate any potential detrimental dopant diffusion along the misfits, preventing the high off-state leakage problem seen in strained-Si/∇_x[$Si_{1-x}Ge_x$]/Si CMOS devices with interfacial misfit dislocations.



(a) (b)

FIGURE 6.12 - Cross-sectional TEM micrographs (a) before and (b) after SiGe and multiple etchstop layer removal.

Clearly, there is significant potential for high-power devices on Si using this method. For example, since the SiGe bonding layer should be fully relaxed, we are free to incorporate previously demonstrated heterostructures on this platform, similar to the fabrication of structures on conventional SiGe buffers (*8, 9, 16-21, 74*). It should be noted, however, that the SiGe layer thickness should not be arbitrarily increased beyond that required to offset the source-drain contacts from the interfacial array due to its relatively low thermal conductivity. To illustrate, the thermal flux Φ_Q through a layer in one-dimension is given by Fourier's Law:

$$\Phi_Q = - k \nabla T \approx - k \frac{\Delta T}{d} \qquad \textbf{[6.4]}$$

where k is the thermal conductivity of the layer, ∇T is the temperature gradient in the layer, ΔT is the temperature difference across the layer, and d is the thickness of the layer. (*93*) Thus the ability to draw heat away from the interface is highly dependent on both the material present as well as the thickness of this layer. Specifically, it is the combination of the high d and low k values in conventional SiGe buffers that effectively precludes these structures from high-power applications. For example, relaxed silicon germanium layers with Ge fractions of about 0.25 have significantly reduced thermal conductivities relative to silicon, with values on the order of 0.1 W cm^{-1} K^{-1} at 300 K. (*94*) Thus the thermal conductivity of $Si_{0.75}Ge_{0.25}$ alloy is comparable to an oxide layer (thermal conductivity value of 0.014 W cm^{-1} K^{-1} at 300 K) and would ordinarily serve to significantly reduce heat extraction from the device channel. (*95*) However, by effectively reducing the thickness of the buffer layer from several microns to tens of nanometers, the thermal flux in SGOS is significantly enhanced thereby drastically reducing the propensity for the self-heating effect with this platform. This enhanced thermal conductivity relative to conventional SiGe buffer layers should result in a suppression of local temperature increases near the active device regions, which in turn will prevent the reduction in mobility as well as drive

current seen in devices fabricated on poorly conducting substrates. (*75*) Furthermore, as the thickness of this SiGe layer is epitaxially-defined, there is considerable control over the thickness of this layer.

Shown in **Figure 6.13** is a PVTEM micrograph of the relaxed $Si_{0.72}Ge_{0.28}$/Si interface after SiGe buffer and multiple etchstop removal. Similar to the SSOS structure, the network of misfit dislocations forms upon bonding and is geometrically necessary due to the differing in-plane lattice constants of strained-Si ($a_{\parallel}$ = 0.549nm for strained-Si on relaxed $Si_{0.72}Ge_{0.28}$) and bulk Si ($a_{\parallel}$ = 0.543 nm). Since the difference in the in-plane lattice spacing is approximately the same in this case for relaxed $Si_{0.76}Ge_{0.24}$ on Si as the previous case for the strained Si layer in SSOS, we would expect the average spacing of the dislocations at this interface to be nearly identical. The observed value of about 40nm exhibited in **Figure 6.13** shows that this is indeed the case.

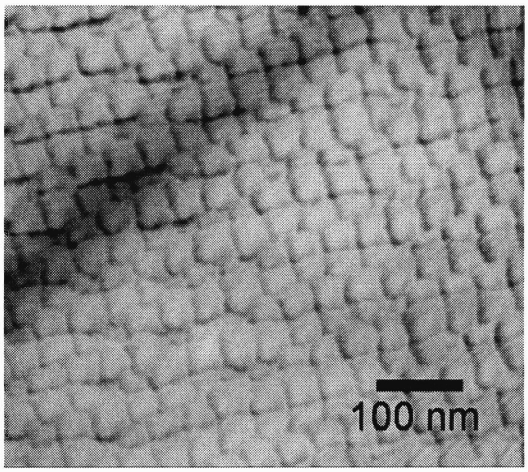
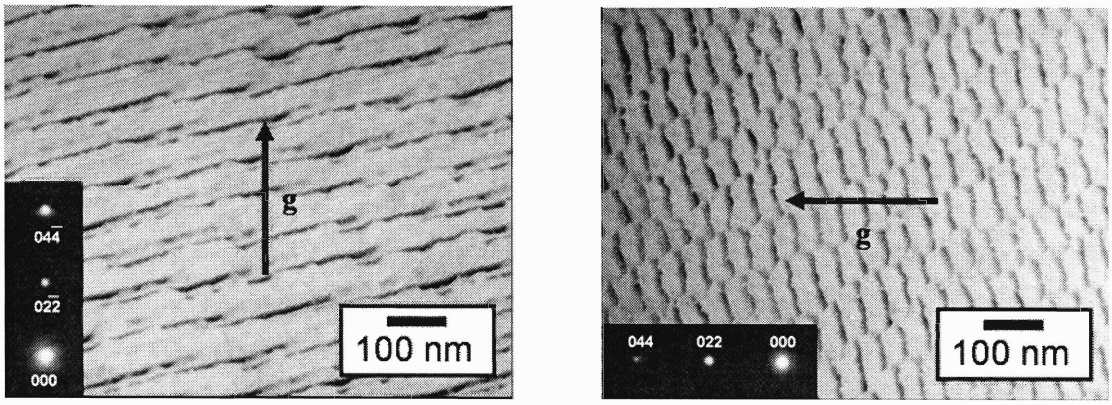


FIGURE 6.13 - Plan-view TEM micrograph showing the misfit array at the bonded relaxed SiGe/Si interface.

Plan-view TEM micrographs from the relaxed SiGe/Si interface are presented in **Figure 6.14** under various 2-beam conditions. Similar to SSOS, the SGOS sample also demonstrates an orthogonal array of edge-type dislocations. The same physics apply for this case, and since the in-plane lattice spacing is the same for relaxed SiGe as for strained-Si, the dislocation structure and

spacing is expected to be nearly identical to the SSOS structure. The twist angle between the layers, θ, was found via asymmetric {224} triple-axis x-ray diffraction to be approximately 0.34°. Substituting the values of the in-plane lattice constants of the bonded layers and the twist angle of 0.34° into **Eqn. 6.3** results in a calculated dislocation spacing of 43.7 nm, in excellent agreement with the spacing of the [110]-type dislocation array exhibited in **Figures 6.13** and **6.14**.



(a) (b)

FIGURE 6.14 – A series of plan view TEM micrographs of the relaxed SiGe/Si interface taken using different g directions for Burgers vector analysis of the dislocation network: (a) g=04-4 and (b) g=044 conditions.

By keeping the SiGe layer thin enough to maintain a high overall thermal conductivity in the structure, yet thick enough to prevent overlap of the source-drain contact with the interfacial misfit array, SGOS would be a very useful platform for high-power MOS applications. Based upon previous determinations of band alignments of similar structures, the expected bandstructure of the SGOS platform is presented in **Figure 6.15**.

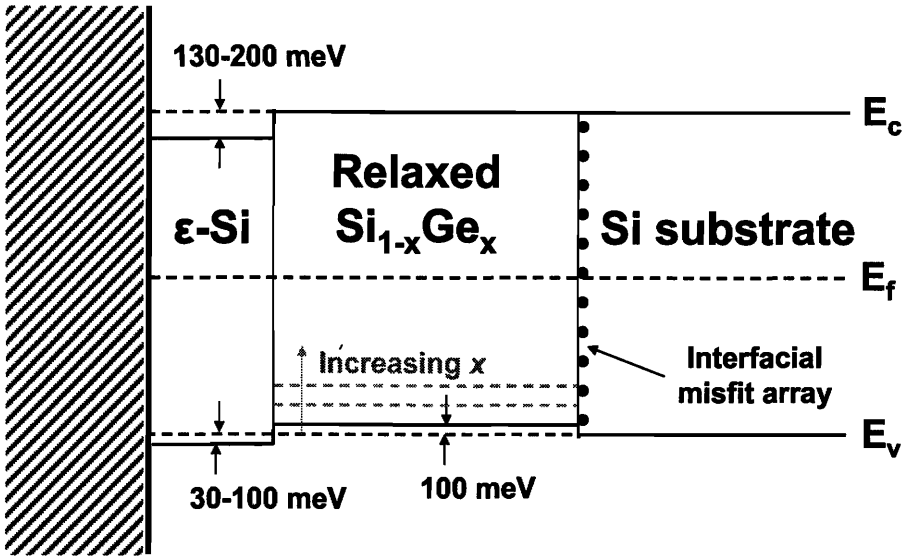


FIGURE 6.15 – Schematic of the expected internal band alignment of the undoped strained-Si on silicon-germanium on Si (SGOS) heterostructure. Values shown are for $Si_{1-x}Ge_x$ with x~0.25. The interfacial misfit array is shown to illustrate its relative location in the structure, not to imply a distribution of levels.

We note that one could further extend this method to utilize a compressively-strained SiGe layer in between the strained and bulk Si layers, thereby providing an enhanced mobility path for holes and making such layers useful for PMOS devices. In this way, dual channel devices can be fabricated for high-power CMOS on this platform, similar to previous structures fabricated directly on relaxed SiGe [**7-8**]. A possible bandstructure of such a platform is presented in **Figure 6.16**.

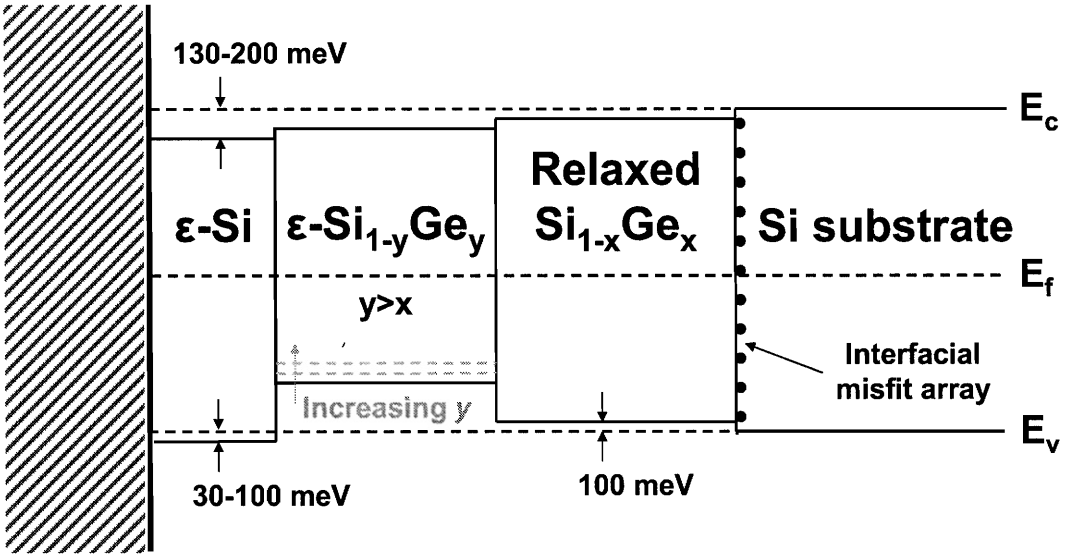


FIGURE 6.16 – Schematic of the expected internal band alignment of an advanced undoped strained-Si on silicon-germanium on Si heterostructure. Values shown are for $Si_{1-x}Ge_x$ with x~0.25. The interfacial misfit array is shown to illustrate its relative location in the structure, not to imply a distribution of levels.

6.6 ULTRATHIN SILICON-GERMANIUM-ON-SILICON

In another embodiment of SGOS, the strained Si layer shown in **Figure 6.10(b)** can be selectively removed. A cross-sectional TEM micrograph of such a structure is shown in **Figure 6.17**. This resulting structure removes several microns of graded material as well as the thick uniform cap layer typically present in conventional graded buffers. In addition, as this layer was lattice-matched to the relaxed SiGe buffer from which it was grown, the layer is expected to be essentially fully relaxed.

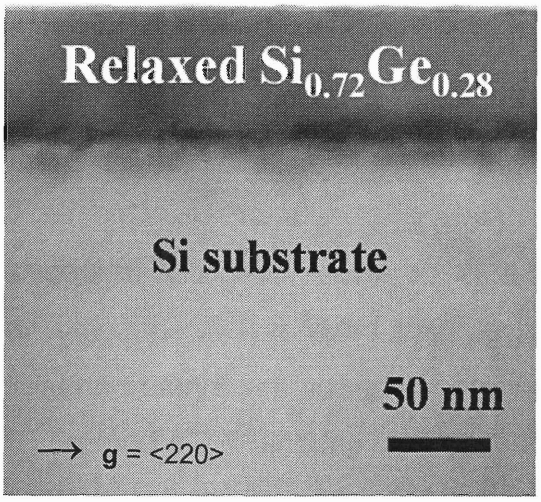


FIGURE 6.17 - Cross-sectional TEM micrograph of an ultrathin relaxed SiGe layer transferred directly to Si.

Raman analysis (λ=514nm) was performed to directly determine if the degree of relaxation in the transferred SiGe layer was equivalent to that of the relaxed SiGe cap layer on which it was grown. Spectra from these samples and a control Si wafer are shown in **Figure 6.18**. The lack of a peak shift in the Raman peak positions indicates that the transferred SiGe layer is indeed fully relaxed.

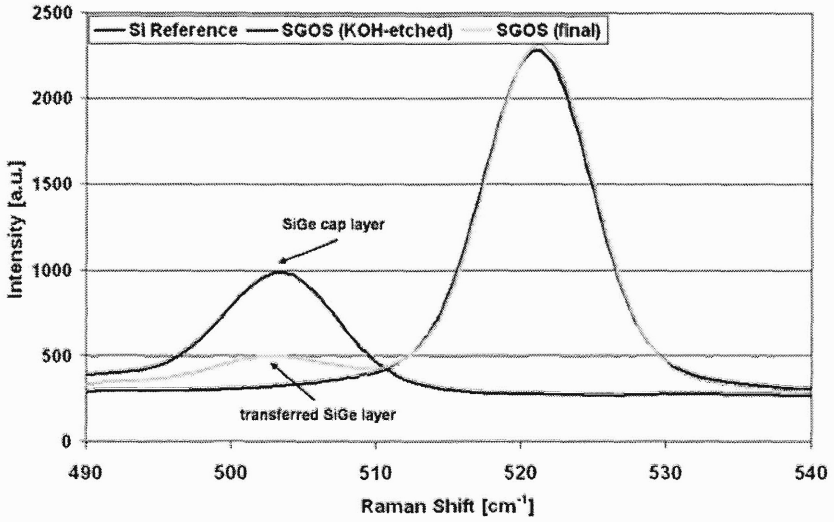


FIGURE 6.18 – Raman spectra of the final SGOS structure as well as prior to SiGe cap and etchstop removal.

As this indicates that a strained-Si channel of sub-critical thickness on this platform would necessarily be fully strained, it is reasonable to assume that the thermal stability of a strained-Si layer grown on this structure would be identical to that grown directly on conventional $\nabla_x[Si_{1-x}Ge_x]$/Si buffers. In this way, the remaining ultrathin relaxed SiGe layer on Si could be used as an enhanced virtual substrate, i.e. it is otherwise identical to conventional $\nabla_x[Si_{1-x}Ge_x]$/Si buffers apart from its reduced thickness. Accordingly, this structure could be used for the subsequent growth of the single- and dual-channel structures previously demonstrated on conventional SiGe buffers, (*8, 9, 16-21, 74*) albeit with a significantly enhanced thermal conductivity near the device region.

6.7 CONCLUSION

Two novel semiconductor platforms, strained silicon-on-silicon (SSOS) and silicon germanium-on-silicon (SGOS), were presented. SSOS substrate has an epitaxially-defined, strained silicon layer directly on bulk silicon wafer without an intermediate SiGe or oxide layer. PVTEM revealed a network of misfit dislocations with an average spacing of approximately 40 nm for this structure, corresponding to the full difference in lattice constant between 0.94% strained Si and relaxed bulk Si, respectively. SSOS substrate is interesting in that a *lack* of misfit dislocations would imply relaxation, in contrast with conventional strained heterostructures. The retention of strain implied by the array of edge dislocations at the interface, coupled to the fact that SSOS is entirely composed of silicon, makes this the first report of a *homochemical heterojunction*. Homochemical heterojunctions are a class of materials which exhibit bandstructure offsets due to differences solely in the strain state, not due to changes in composition as are conventionally achieved.

Silicon germanium-on-silicon (SGOS) substrate utilizes a thin layer of SiGe to separate a strained-Si device channel from a bulk Si substrate. Specifically, this epitaxially-defined SiGe layer serves to distance the source and

drain contacts from the interfacial array, thereby eliminating the off-state leakage problem SSOS would likely exhibit. Furthermore, by distancing the interfacial array from the overlying etching surface, preferential etching of dislocation is minimized, considerably simplifying substrate fabrication. Raman spectroscopy indicated that the transferred SiGe layer is fully relaxed, and therefore any strained Si channel of sub-critical thickness on this platform would necessarily be fully strained.

CHAPTER 7: ADVANCED DONOR STRUCTURES FOR STRAINED-SILICON LAYER TRANSFER

"Hee hee. 'Get her.' That was your whole plan? I like it; it was scientific."

- Dr. Peter Venkman

7.1 INTRODUCTION

At present, there is considerable interest in the development of engineered substrates, i.e. substrates with added value and functionality as compared to conventional bulk substrates such as Si and GaAs. (*96*) Notable examples now under active development include strained silicon-on-insulator (SSOI) (*72, 97*) and germanium-on-insulator (GOI). (*73, 98*) SSOI and GOI substrates are attractive platforms for future generations of complimentary metal-oxide-semiconductor (CMOS) devices owing to their significantly enhanced carrier mobility values relative to bulk Si and the reduction in parasitic capacitance offered by the on-insulator (OI) platform. However, a noteworthy impediment to the widespread adoption of either of these platforms is that they require a scaleable as well as cost-effective donor platform from which thin strained-Si and Ge layers can be efficiently transferred to large-diameter Si handle wafers. To create relaxed lattice constants of SiGe on Si with low threading dislocation densities in the surface layer, the relaxed graded SiGe buffer (i.e. $\nabla_x[Si_{1-x}Ge_x]/Si$) (*8, 9, 14*) has been utilized for both the SSOI as well as GOI platforms. This $\nabla_x[Si_{1-x}Ge_x]/Si$ structure allows for the realization of an arbitrary lattice constant between that of bulk Si and Ge, thereby allowing for thin layers of Si, Ge, and SiGe to be transferred in either a strained or relaxed state.

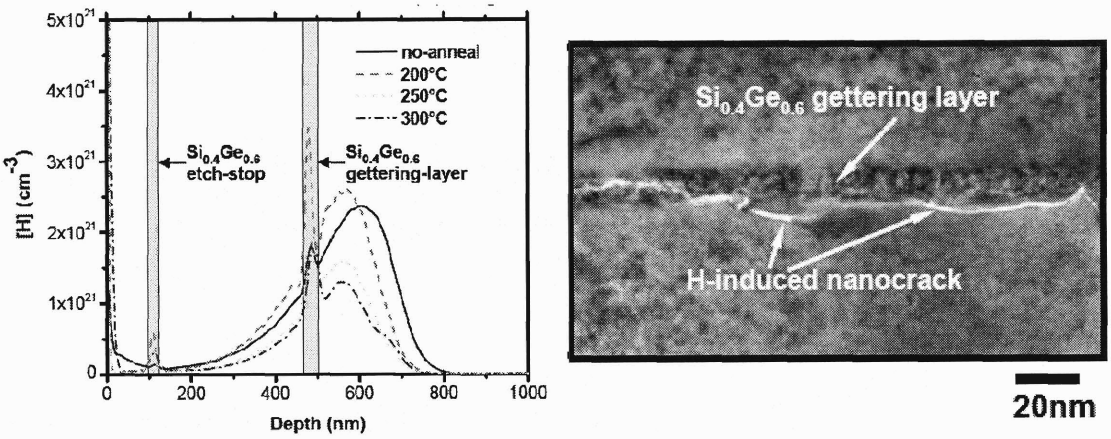
In this work, we have investigated the application of buried strained-Si layers in $\nabla_x[Si_{1-x}Ge_x]/Si$ structures to improve the fabrication of SSOI substrate. Our goals are to investigate H-gettering in strained-Si layers for enhanced exfoliation and to thereby investigate structures incorporating strained-Si layers to potentially re-use $\nabla_x[Si_{1-x}Ge_x]/Si$ template wafers.

7.2 HYDROGEN GETTERING IN TENSILELY STRAINED LAYERS

Relatively large doses of implanted hydrogen are required to induce splitting via the hydrogen-exfoliation process. (*66, 99*) The dose required for

splitting depends on the composition of the layer in which splitting is induced; (*100*) however, for all substrate materials the cost of implantation is dependent on the dose required. Thus, there is a continual interest in reducing the implantation dose and therefore cost of layer transfer.

Enhanced gettering of H has been observed in tensile high-Ge content epitaxial layers. In the work of Pitera *et al.*, a buried, tensilely strained $Si_{0.4}Ge_{0.6}$ layer in relaxed Ge on Si (i.e. $Ge/\nabla_x[Si_{1-x}Ge_x]/Si$) demonstrated significant gettering of implanted hydrogen relative to surrounding relaxed Ge layers, thus greatly simplifying the fabrication of GOI substrate, as shown in **Figure 7.1**. (*101*)



(a) **(b)**

FIGURE 7.1 – (a) SIMS results showing hydrogen gettering in tensilely strained $Si_{0.4}Ge_{0.6}$ layers in relaxed Ge and (b) XTEM image showing nanocracks preferentially forming in the gettering layer. Note in (a) that each $Si_{0.4}Ge_{0.6}$ layer within the structure getters hydrogen. Images courtesy of A. J. Pitera. (*13*)

The primary hydrogen gettering mechanism in that work was the nucleation of platelets within the $Si_{0.4}Ge_{0.6}$ layer. While the formation of {111}-type platelets with a concomitant local accumulation of hydrogen in ion-implanted bulk semiconductors is a well known phenomenon, the work of Pitera *et al.* demonstrated a significant density of platelets with {100}-type habit planes.

These {100}-type platelets were determined to have preferentially formed in order to relax the biaxial tensile strain in the $Si_{0.4}Ge_{0.6}$ layer and simultaneously getter hydrogen, thereby considerably improving the layer transfer process. A schematic of the means by which these platelets can partially relieve biaxial tensile stress is shown in **Figure 7.2**.

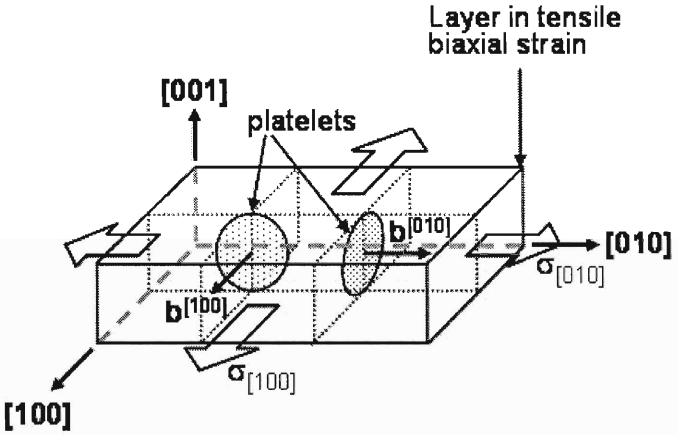


FIGURE 7.2 – Schematic of homogeneously-nucleated circular (100) and (010) platelets within a (001)-oriented layer in biaxial tension. Image courtesy of A. J. Pitera. (*13*)

Furthermore, tensile strain can allow for an increase in the solubility of interstitial hydrogen relative to otherwise equivalent relaxed or compressively strained material. This is due to the fact that the introduction of an interstitial impurity atom into a crystal is associated with a local dilation of the surrounding lattice. The energy associated with this process is related to the specific volume of the impurity atom, $\overline{V}_{H_2{}^i}$, as well as the stress state in the vicinity of the interstitial site. Accordingly, the energy associated with an interstitially-dissolved hydrogen molecule is given by $-P\overline{V}_{H_2{}^i}$. The applied pressure, P, can be expressed in terms of the principal stress components as $-(\sigma_{xx}+\sigma_{yy}+\sigma_{zz})/3$. For a layer under biaxial stress, $\sigma_{xx}=\sigma_{yy}$ and $\sigma_{zz}=\theta$ Therefore, the solubility of interstitial hydrogen in a layer experiencing a biaxial tensile strain, ε, is altered

according to **Eqn. 7.1** where $[H_2{}^i]_0$ is the solubility in the absence of strain, M is the biaxial modulus of elasticity, k_B is Boltzmann's constant and T is the absolute temperature.

$$[H_2{}^i](\varepsilon) = [H_2{}^i]_0 \exp\left[\frac{2\varepsilon M \overline{V}_{H_2{}^i}}{3k_B T}\right] \qquad \textbf{[7.1]}$$

Since interstitial hydrogen creates a dilation of the surrounding lattice, $\overline{V}_{H_2{}^i}$ is always a positive value. Therefore tensile strain ($\varepsilon > 0$) is expected to cause an exponential increase of H solubility while compression ($\varepsilon < 0$) has the opposite effect. (*102*)

Tensile strain should therefore serve to aid layer transfer processes for multiple reasons. The increased solubility of H results in the concentration of H in thin layers specified by epilayer location. Platelet formation results in further gettering of hydrogen on {100}-type planes. As a result, the hydrogen implant is effectively further focused within the layer, thereby potentially reducing the required dose (and therefore cost) of implantation. The formation of these platelets provides a sink for supersaturated hydrogen to come out of solution in the surrounding lattice. As a result, the platelets pressurize with molecular hydrogen and therefore the location of splitting can be determined with greater precision than would otherwise be achieved.

In this work, we attempt to determine if a similar hydrogen gettering method occurs within pure tensile Si, as opposed to tensile Ge-rich layers. Additionally, multiple distributed strained-Si layers were incorporated in each structure in order to study the influence of increases in both damage as well as H concentration, thereby potentially elucidating the platelet formation mechanism in tensilely strained layers with a single implant.

7.3 BURIED STRAINED-SILICON ETCHSTOP LAYERS

To date, the process of layer transfer for the fabrication of engineered substrates such as SSOI and GOI has been non-conservative, i.e. the original $\nabla_x[Si_{1-x}Ge_x]$/Si donor structure is typically discarded after layer transfer. Re-use of much of the processing incorporated into these donor structures is desirable. Although tensile silicon layers are investigated for H gettering in this work, we also incorporate other strained-Si layers to serve as etchstop layers to aid in deriving a process which can re-use the $\nabla_x[Si_{1-x}Ge_x]$/Si donor wafers.

Strained-Si has been utilized as a chemically-selective etch-stop layer relative to SiGe in the fabrication of silicon germanium-on-insulator (SGOI) (*69, 70, 103*), SSOI (*72*), as well as strained silicon-on-silicon (SSOS) and silicon germanium-on-silicon (SGOS) (*86, 104*) substrates. A novel extension of this previous work would therefore involve utilizing ε-Si layers within the structure to serve not only as transfer and H-gettering layers, but also as a selective etchstop layer within the structure. After splitting via hydrogen-induced layer exfoliation, the surface of the donor substrate would exhibit a significantly damaged surface composed of a portion of the remaining ε-Si gettering layer and/or relaxed SiGe. By employing selective SiGe etch chemistries, such as HNO_3:HAc:dHF (*69*), the damaged region could be selectively removed, leaving a ε-Si/$\nabla_x[Si_{1-x}Ge_x]$/Si structure with a smooth surface. Similarly, the damaged SiGe layer could be selectively removed using a low-temperature wet oxidation step followed by immersion in a dilute HF solution. (*72*) Regardless of the SiGe removal method used, the remaining ε-Si/$\nabla_x[Si_{1-x}Ge_x]$/Si structure could then be re-used by re-growing the donor structure and beginning the implantation and transfer process anew.

7.4 RE-USE OF DONOR $\nabla_x[Si_{1-x}Ge_x]$/Si WAFERS USING STRAINED-SI FOR H-GETTERING AND ETCHSTOP LAYERS

A generalized process flow which could utilize strained-Si layers for the re-use of a significant portion of a SSOI donor structure is shown in **Figure 7.3**. As shown in **Figure 7.3(a),** a $\nabla_x[Si_{1-x}Ge_x]$/Si structure would be graded out to a terminal SiGe composition and subsequently chemical mechanical polished (CMPed) to reduce the characteristic crosshatch pattern. A transfer structure utilizing the aforementioned strained-Si etchstop, H-gettering, and transfer layers would then be grown at reduced temperatures to preserve planarity at the surface. After deposition of an oxide screening layer, the structure would then be implanted with hydrogen at a depth slightly below the hydrogen gettering layer, as shown in **Figure 7.3(b)**. (*68*) This donor structure would then be bonded to a Si handle wafer and subsequently annealed to induce layer exfoliation, leaving the donor structure as shown in **Figure 7.3(c)**. Any remaining Si could then be removed via a brief immersion in either a tetramethylammonium hydroxide (TMAH) or KOH solution, followed by a SiGe-selective etch such as that developed by Taraschi *et al.* (*105*) Stopping on the strained-Si etchstop would leave the structure as shown in **Figure 7.3(d)**, at which point the transfer structure could then be regrown to the state of **Figure 7.3(a)** allowing the process to be continued anew. Such a process would therefore allow for the re-use of the original substrate, graded buffer growth, as well as the CMP step of the SiGe cap.

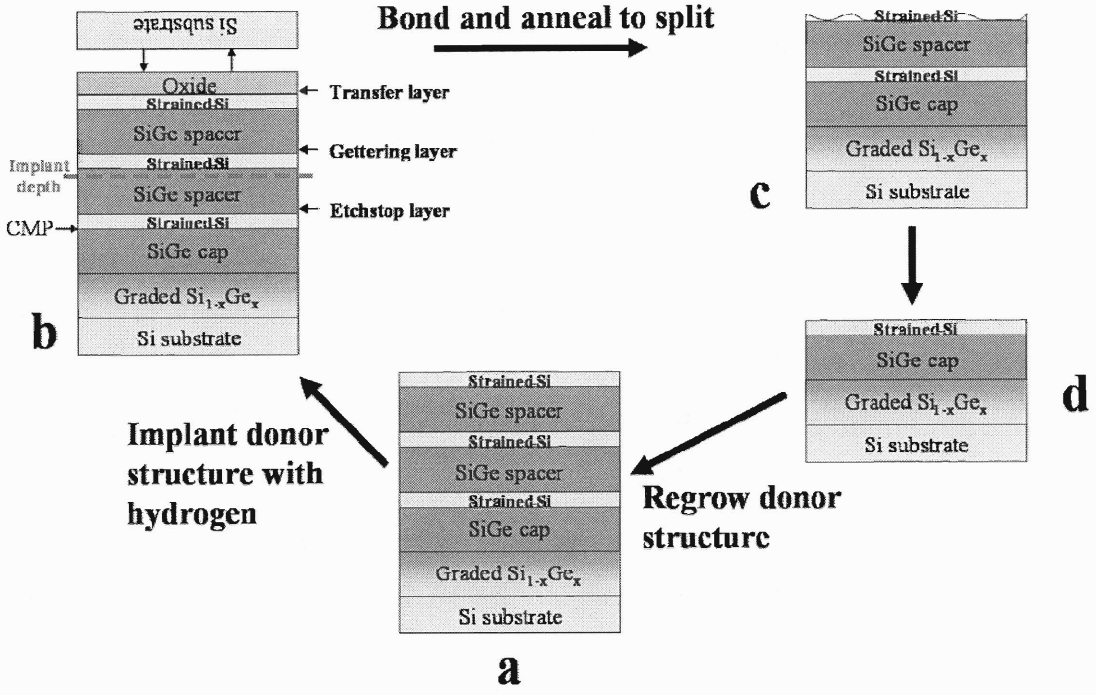


FIGURE 7.3 – Generalized process flow for the re-use of relaxed graded SiGe donor structures utilizing strained-Si transfer, gettering, and etchstop layers.

With these goals in mind, we design a set of experiments to determine if buried tensile strained-Si layers can be successfully applied to the potential re-use of $\nabla_x[Si_{1-x}Ge_x]$/Si donor structures for SSOI substrate development. Accordingly, the goals of this study will be to determine the H-gettering ability of strained-Si layers and to demonstrate the process outlined above up to the state shown in **Figure 7.3(d)**.

7.5 EXPERIMENTAL OVERVIEW

The experimental structures utilized in this work involved growth of relaxed graded SiGe buffers on 150mm Si(001) substrates via ultra-high vacuum chemical vapor deposition (UHVCVD) at 900 °C, which were graded at 10% Ge μm^{-1} to final compositions of approximately 25, 40, and 50% Ge. These compositions were selected in order to achieve approximately 1, 1.6, and 2% tensile strain, respectively, in the subsequent growth of Si layers. The

combination of a low grading rate and a high growth temperature results in essentially complete relaxation with a threading dislocation density of approximately 10^5 cm^{-2}. (*28*) Deposition of the experimental H-gettering structures, comprised of a series of distributed strained-Si layers separated by relaxed SiGe spacer layers, then occurred at 550 °C in order to suppress surface roughening. A distribution of strained-Si layers was included in each of the structures in order to study the gettering of strained-Si as a function of local H-content. As misfit dislocations can also getter hydrogen, the thickness values of the strained-Si layers were chosen to be approximately the critical thickness for each structure. This precludes the possibility for H-gettering via the formation of misfit dislocations at the interfaces. An additional strained-Si layer, located beneath the experimental H-gettering structure, was included as an etchstop layer to explore the potential for re-using a significant portion of the donor structure. Cross-sectional transmission electron microscopy (XTEM) images of the as-grown structures used for this study are shown in **Figure 7.4**.

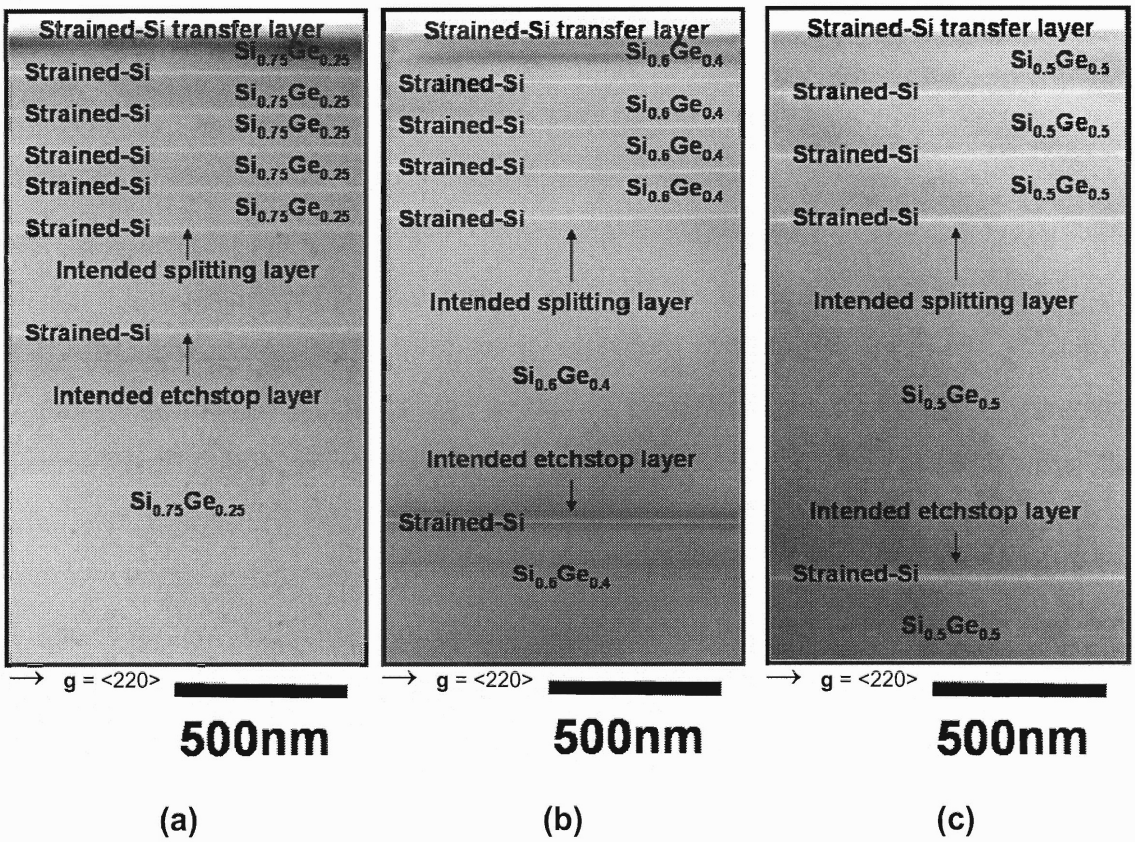


FIGURE 7.4 – Cross-sectional TEM micrographs of the various tensilely strained-Si gettering structures used in this study. The Ge concentrations are (a) 25% Ge, (b) 40% Ge, and (c) 50% Ge to introduce 1, 1.6, and 2% tensile strain in Si layers, respectively.

The above structures were implanted with protons (H^+) at room temperature to a dose of 6×10^{16} cm^{-2} at 80 keV. Cross-sectional TEM images of the as-implanted structures are shown in **Figure 7.5.**

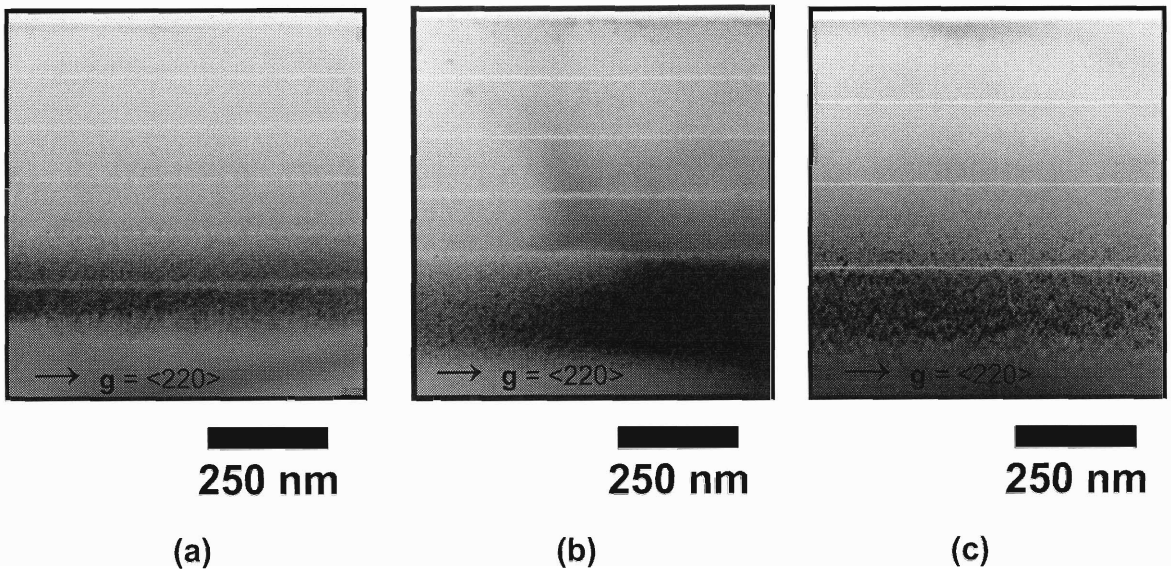


FIGURE 7.5 – Cross-sectional TEM micrographs of the various tensilely strained-Si gettering structures used in this study in the as-implanted condition. The Ge concentrations are (a) 25% Ge, (b) 40% Ge, and (c) 50% Ge.

Cross-sectional transmission electron microscopy (XTEM), using JEOL 2010FX and 2000FX microscopes, was performed in order to the study the microstructure of the heterostructures as a function of post-implant annealing. TEM samples were prepared for imaging along the standard [110]-pole as well as the [100]-pole for defect-specific contrast. Secondary ion mass spectroscopy (SIMS) was utilized to determine the hydrogen and germanium profiles in the structures. Rutherford backscattering spectrometry (RBS) with [100] ion channeling using a 2.275 MeV He^{++} ion beam was used to explore the damage profile of each structure. Ex-situ annealing took place under flowing N_2.

Lastly, in order to cause surface blistering and therefore demonstrate the layer transfer properties, the experimental structures in this study were annealed at various temperatures. We note here that the surface blistering behavior of annealed, H-implanted Si has been directly correlated with the location of splitting during wafer bonding and layer transfer. (*106*) This allows for a direct

extension of the surface blistering behavior of the structures in this study to the layer exfoliation behavior of commercial strained-Si layer transfer applications.

7.6 HYDROGEN REDISTRIBUTION AND PLATELET EVOLUTION IN H^+-IMPLANTED STRAINED-SILICON LAYERS

Shown in **Figures 7.6-7.8** are the H profiles in each of the samples after implantation as well as after annealing at 300°C for 1 hour. This temperature was empirically determined to result in a redistribution of H, but not layer exfoliation. As can be seen in the **Figures**, the relative gettering efficiency of the deepest strained-Si layers, i.e. the intended splitting layers, increases with the value of strain within the structures. Additionally, the level of H accumulated in the strained-Si layers within each structure increases with depth. It is interesting to note that in the work of Pitera *et al.,* (*101*) all tensilely strained layers gettered significant amounts of hydrogen, as indicated by a single peak being observed for each ε-$Si_{0.4}Ge_{0.6}$ layer. As seen in **Figures 7.6-7.8**, however, in the low H-content regions for each sample, H-gettering actually occurs at the periphery of the strained-Si layers.

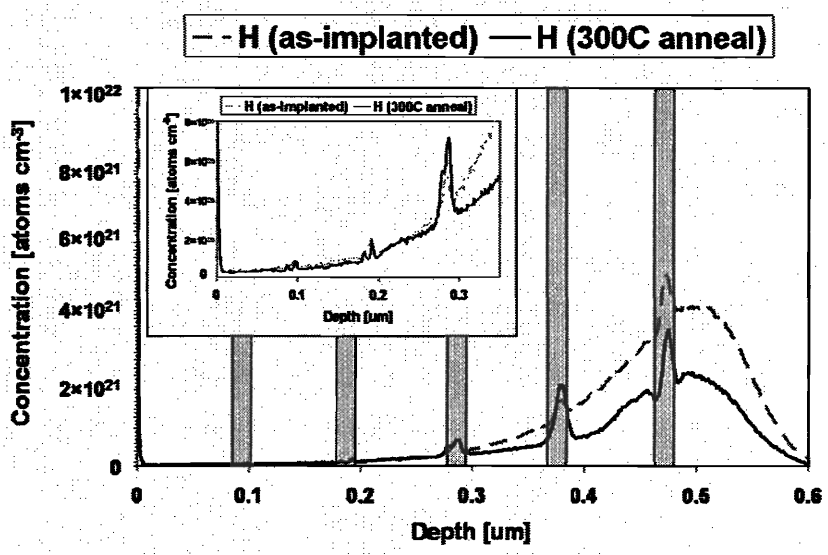


FIGURE 7.6 – Hydrogen SIMS data of the implanted $Si_{0.75}Ge_{0.25}$-based structure showing as-implanted and post-annealed concentrations. Shaded regions indicate the location of tensilely strained Si layers. Shown in the inset is an expanded view of the region with low local H-content.

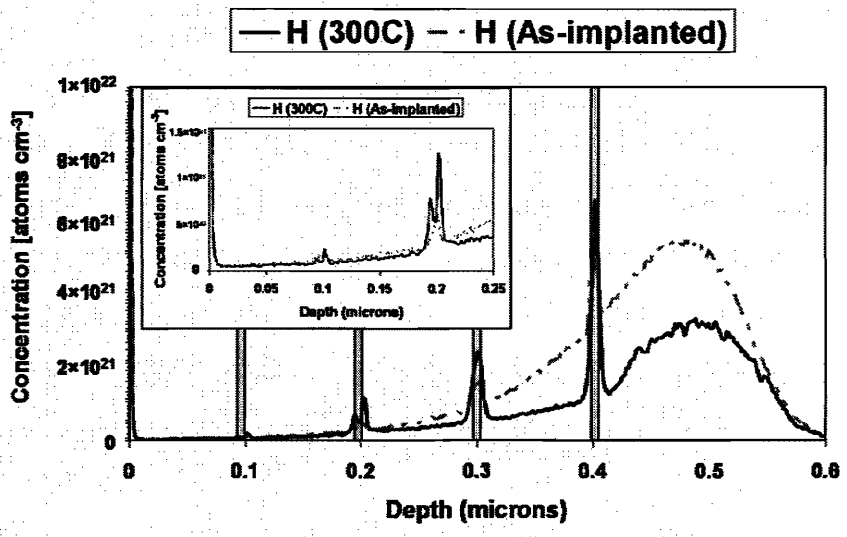


FIGURE 7.7 – Hydrogen SIMS data of the implanted $Si_{0.6}Ge_{0.4}$-based structure showing as-implanted and post-annealed concentrations. Shaded regions indicate the location of tensilely strained Si layers. Shown in the inset is an expanded view of the region with low local H-content.

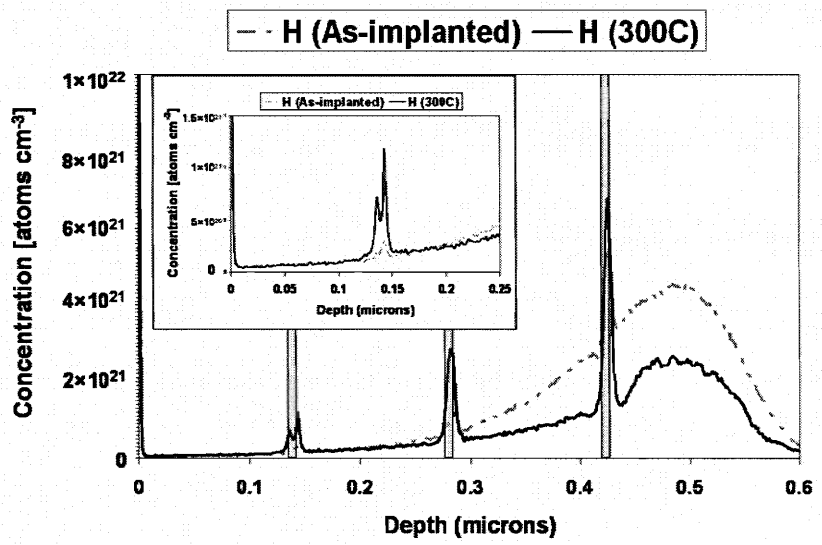


FIGURE 7.8 – Hydrogen SIMS data of the implanted $Si_{0.5}Ge_{0.5}$-based structure showing as-implanted and post-annealed concentrations. Shaded regions indicate the location of tensilely strained Si layers. Shown in the inset is an expanded view of the region with low local H-content.

For the case of a high local hydrogen concentration, significant gettering occurs within the tensile strained-Si layers, as exhibited via SIMS by the existence of a single peak for each layer. Shown in **Figure 7.9** is a plot of the relative enhancement in H concentration as a function of strain for the two deepest strained-Si layers in each of the structures in both the as-implanted and post-annealed conditions. The relative H-gettering enhancement is defined as the ratio of the peak H concentration in a strained-Si layer to its surrounding SiGe matrix. The H concentration of the surrounding SiGe is defined as the average of the H concentrations immediately adjacent to the strained-Si layers.

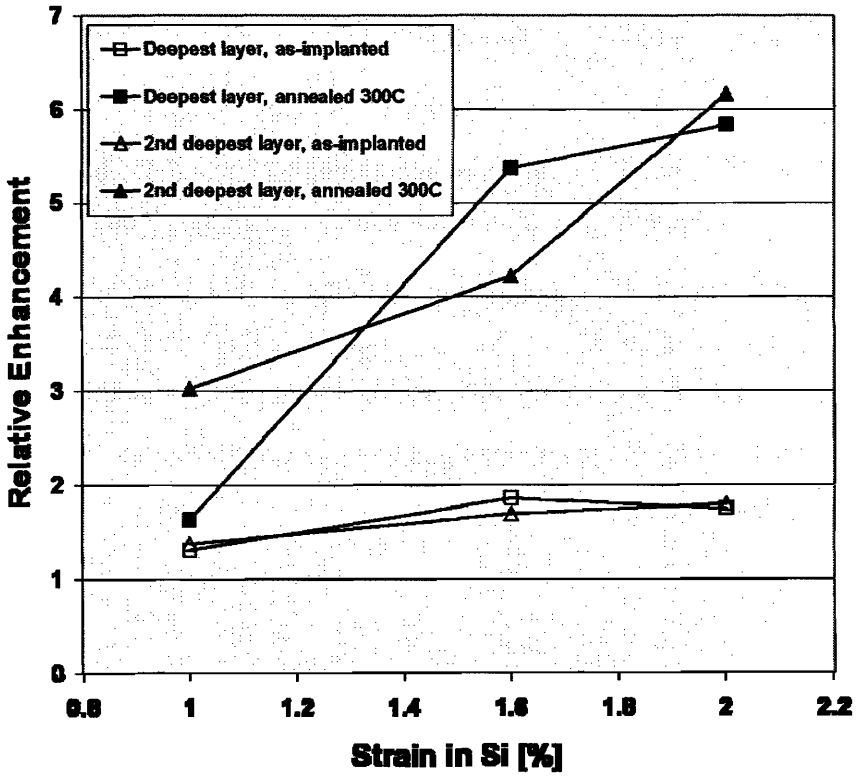


FIGURE 7.9 – Plot of relative H-gettering enhancement in strained-Si relative to adjacent SiGe as a function of strain. Note the strong dependencies on both the level of strain as well as annealing.

As shown in **Figure 7.9**, in general the relative H-gettering enhancement of the strained-Si layers are fairly low (~1.3-1.9×) in the as-implanted condition, with significant enhancements observed after annealing at 300°C for 1 hour. However, the 1% tensile strained-Si shows particularly interesting behavior in that the gettering enhancement of the deepest layer after annealing at 300°C is comparable to its as-implanted condition. Furthermore, the enhancement of this layer is significantly lower than that of the second deepest layer after annealing at 300°C. We believe this to be related to the fact that, in general, the implant damage profile is roughly correlated with the implanted H profile. As such, the relative H-gettering enhancement of the deepest 1% strained-Si layer is hindered by both its relatively low tensile strain level as well as the fact that damage in the adjacent SiGe layers can also trap H. In contrast, the damage in the SiGe layers surrounding the second deepest 1% strained-Si layer is lower, thereby allowing

for a relatively increased H-gettering enhancement for this strained-Si layer despite its similarly low tensile strain level.

The type of H-gettering behavior exhibited by the deepest strained-Si layers in this work has previously been correlated to the formation of {100}-type platelets in tensilely strained $Si_{0.4}Ge_{0.6}$ in relaxed Ge. (*101*) Shown in **Figures 7.10-7.12** are XTEM images of the 25-, 40-, and 50% Ge-based experimental gettering structures after H-implantation and subsequent annealing at 300°C for 1 hour. Each of the samples was imaged along the [100]-pole in order to view the {100}-type platelets edge-on.

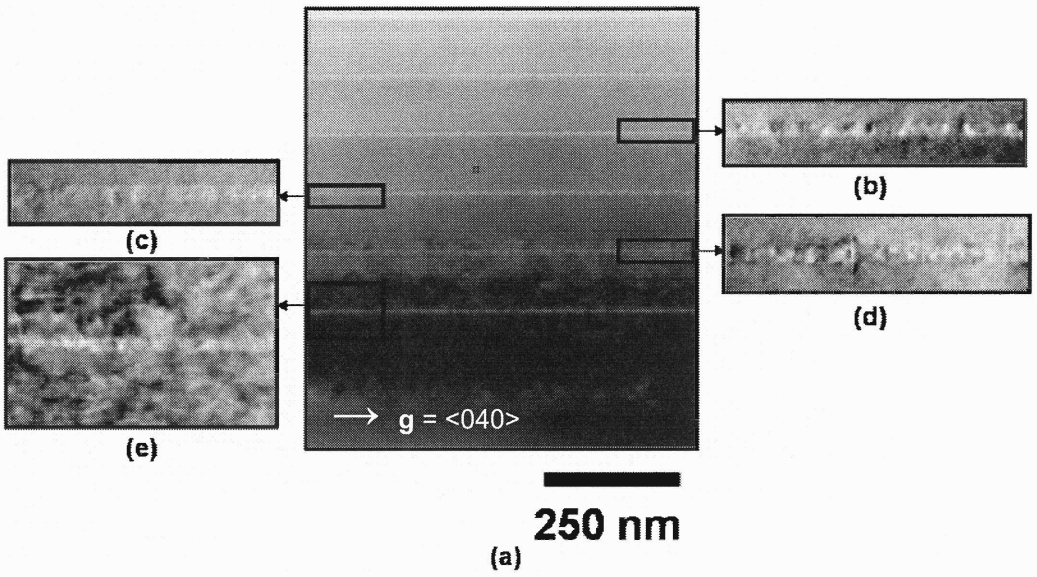


FIGURE 7.10 – Post-implantation XTEM images of the 1% strained-Si structure after annealing at 300°C for 1 hour. Sample was prepared along the [100]-pole to image the {100} platelets edge-on.

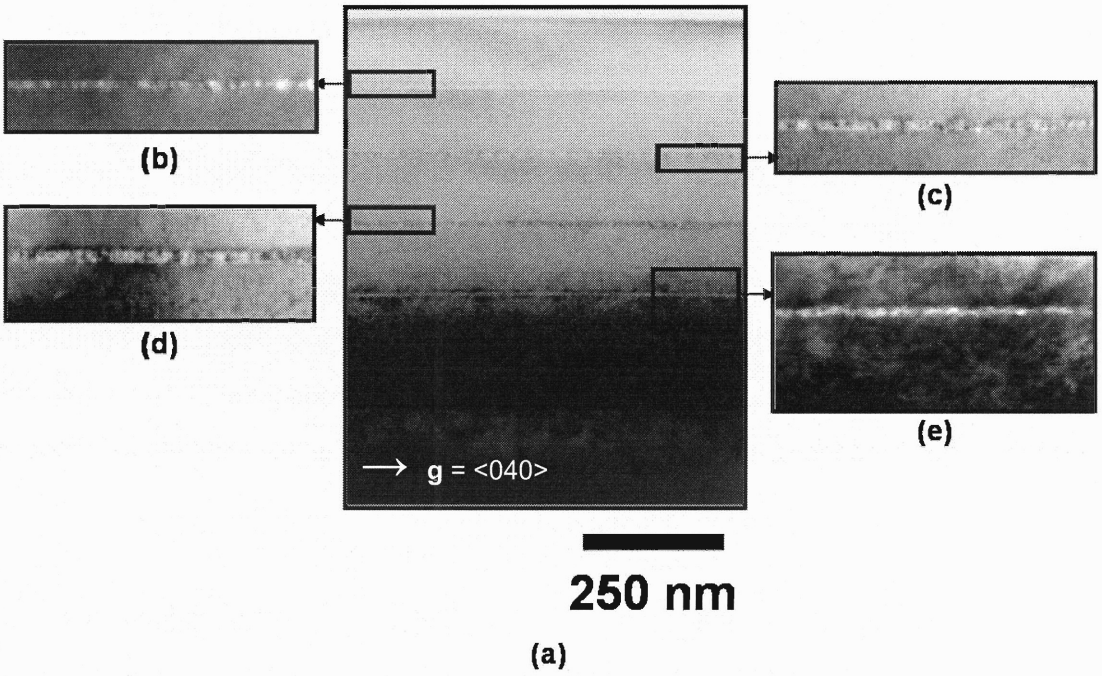


FIGURE 7.11 – Post-implantation XTEM images of the 1.6% strained-Si structure after annealing at 300°C for 1 hour. Sample was prepared along the [100]-pole to image the {100} platelets edge-on.

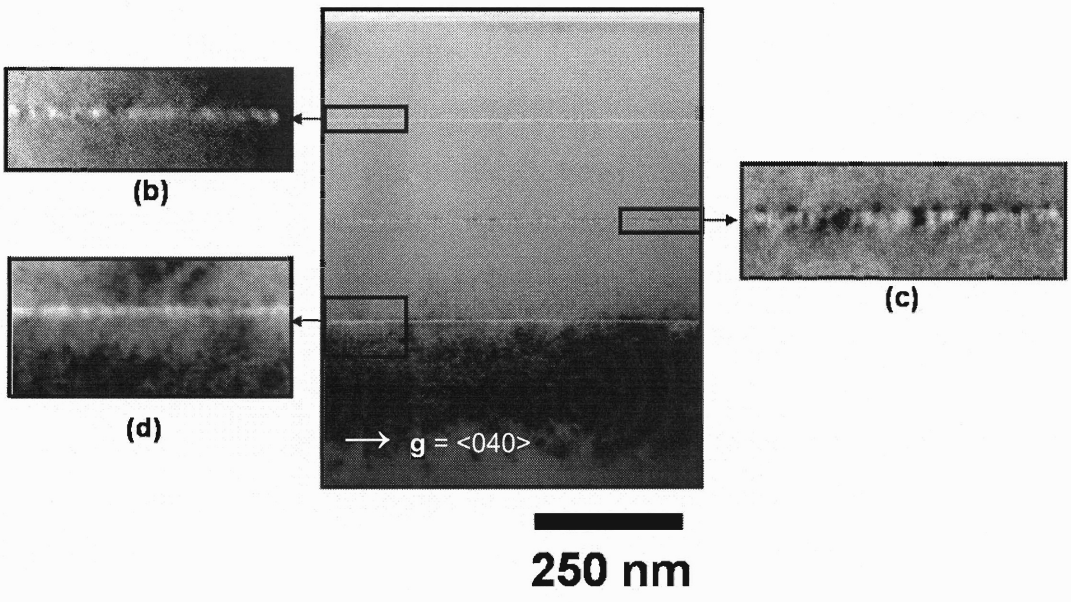


FIGURE 7.12 – Post-implantation XTEM images of the 2% strained-Si structure after annealing at 300°C for 1 hour. Sample was prepared along the [100]-pole to image the {100} platelets edge-on.

As can be seen in **Figures 7.10-7.12**, there are several trends in the evolution of the defect morphologies. Firstly, there is a clear correlation between the local hydrogen concentration and the types of defects observed in each layer. In the uppermost ε-Si layers of each structure, a "speckled" contrast is observed, which appears to coincide spatially with the strained-Si/$Si_{1-x}Ge_x$ interfaces, with few {100}-type platelets spanning the entire strained-Si layers visible. Further into the structures, more platelets appear, with less of the "speckled" contrast seen in the uppermost layers visible. Still further into the structures, extensive {100}-type platelet formation appears to occur exclusively, similar to the work of Pitera *et al.* (*101*)

The "speckled" contrast observed in the uppermost layer(s) of each structure, which has been correlated with SIMS to involve H-gettering at the periphery of the layers, may suggest the mechanism by which platelets nucleate in tensilely strained layers. For example, gettering of H has been seen previously at the Si/SiO_2 interface (*107*). In that work, it was speculated that the accumulation of H at the interface was associated with the bridging of strained Si-Si bonds at the Si/SiO_2 interface. It is possible that a similar mechanism is operating in the embryonic stage of platelet formation.

It has been experimentally determined that the most stable configuration for H in Si is in the bond-centered (BC) configuration. (*108*) The formation of this configuration is driven by the Coulombic attraction of H to the high negative charge density of the Si-Si bond. A theoretical treatment of the accumulation of H via the bridging of tensilely strained Si-Si bonds in the BC configuration was treated well by Van de Walle and Nickel. (*109*) In that work, it was determined that while the energy gain associated with H entering a Si-Si bond in a strained-Si layer to form a partially relaxed Si-H-Si bond would be approximately the same as H entering a Si-Si bond in relaxed Si, the energy cost associated with forming the new bond configuration would decrease with the degree of tensile strain. As a result, Van de Walle and Nickel calculated the energy level of H incorporation

into a strained Si-Si bond to be approximately 0.25-0.55 eV lower than that of H incorporation into an originally relaxed Si-Si bond, making such a configuration significantly more stable.

As such, it is to be expected that for the case that the local H concentration is too low to form strain-relieving platelets, yet the diffusivity of H is high due to a lack of local implantation damage, mobile H diffusing within the surrounding relaxed $Si_{1-x}Ge_x$ layers could pileup at the strained-Si/$Si_{1-x}Ge_x$ interfaces in order to relax strained Si-Si bonds and reduce the overall energy of the system. In this way, it would be expected that the amount of interfacial gettering would be proportional to both the local mobile H concentration present as well as the degree of strain in the strained-Si layer. This is exhibited in **Figures 7.6-7.8,** in which the peak concentration of H at the strained-Si/SiGe interfaces increases with the level of strain in the system at equivalent depths. Note also that for each layer, the accumulation of hydrogen is higher on the deeper side of the layer. As the deeper side of each layer is associated with a higher concentration of H and is first to see H diffusing to the surface, this supports the argument outlined above.

For a sufficiently low H-content, there would be no incentive to diffuse further into the layer, resulting in the gettering of H at the interface only. In this way, it is possible that the nucleation of platelets in a tensilely strained layer occurs at the strained-Si/SiGe interface, evolving from H in the BC configuration. Platelet growth would then continue into the strained-Si layer as additional hydrogen diffuses into the layer.

Overall, however, enhancements in H-gettering are observed in the strained-Si layers after annealing as well as with increasing strain levels within the structures. As correlated with XTEM, this H accumulation was determined to occur via the formation of {100}-type strain-relieving platelets, similar to the seminal work of Pitera *et al.* in ε-$Si_{0.4}Ge_{0.6}$ in relaxed Ge/$\nabla_x[Si_{1-x}Ge_x]$/Si. Such

accumulation is promising for lowering the implanted H^+ dose and, hence, cost structure associated with SSOI substrate.

7.7 BLISTERING BEHAVIOR OF STRAINED-SILICON IN RELAXED $Si_{1-x}Ge_x$

While the enhancement in the local hydrogen concentration offered by using tensilely strained Si as a H-gettering layer has been successfully demonstrated, it remains to be shown that such layers are truly useful for enhancing strained-Si layer transfer. Shown in **Figures 7.13-7.15** are representative XTEM and Nomarski optical images of each of the structures after blistering has occurred via annealing for 1 hour each at both 300°C and 500°C. These temperatures were chosen to form the previously described {100}-type platelets and induce layer exfoliation, respectively. As seen in the optical micrographs of **Figure 7.13-7.15(b)**, all samples blister after the aforementioned thermal treatment. However, as shown in the XTEM images of **Figures 7.13-7.15 (a)**, the 40 and 50% Ge-based samples split preferentially along the lowest strained-Si layers, as intended, while the 25% Ge-based sample actually splits around the periphery of the lowest strained-Si layer. This behavior is somewhat unexpected, as it was demonstrated in **Figure 7.6** that the H concentration is highest in that structure within the lowest strained-Si layer.

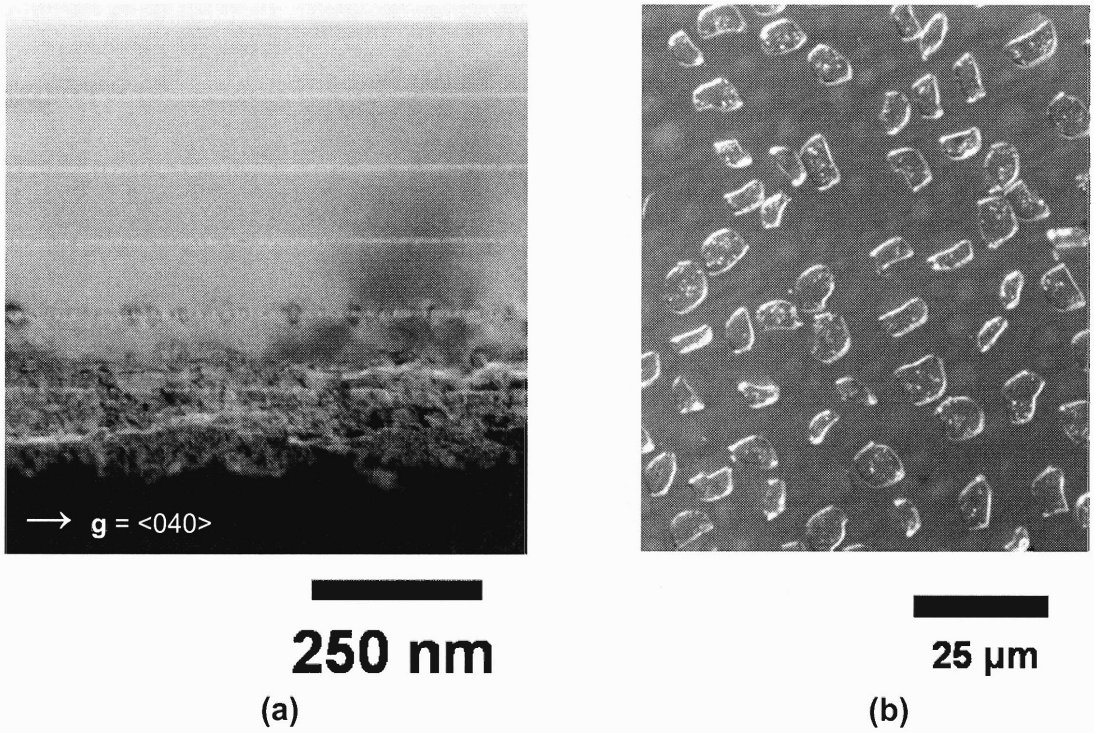


FIGURE 7.13 – (a) XTEM micrograph and (b) Nomarksi optical micrograph of the 25%-based structure after blistering. Note that the XTEM image in (a) is along the [110] pole.

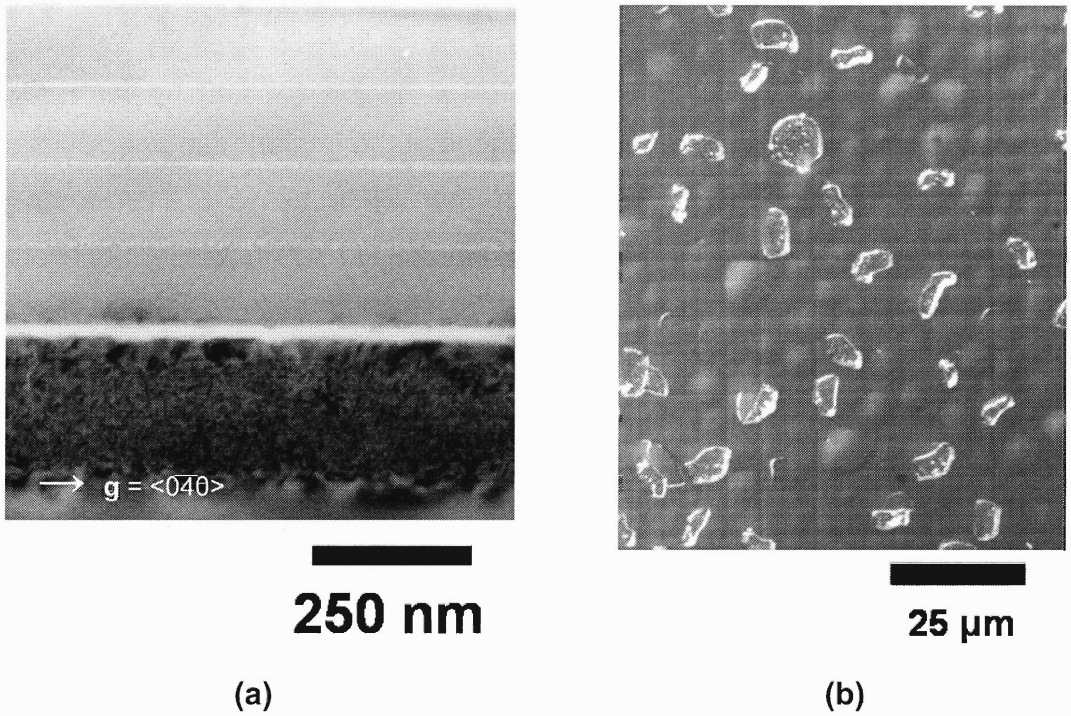


FIGURE 7.14 – (a) XTEM micrograph and (b) Nomarksi optical micrograph of the 25%-based structure after blistering. Note that the XTEM image in (a) is along the [110] pole.

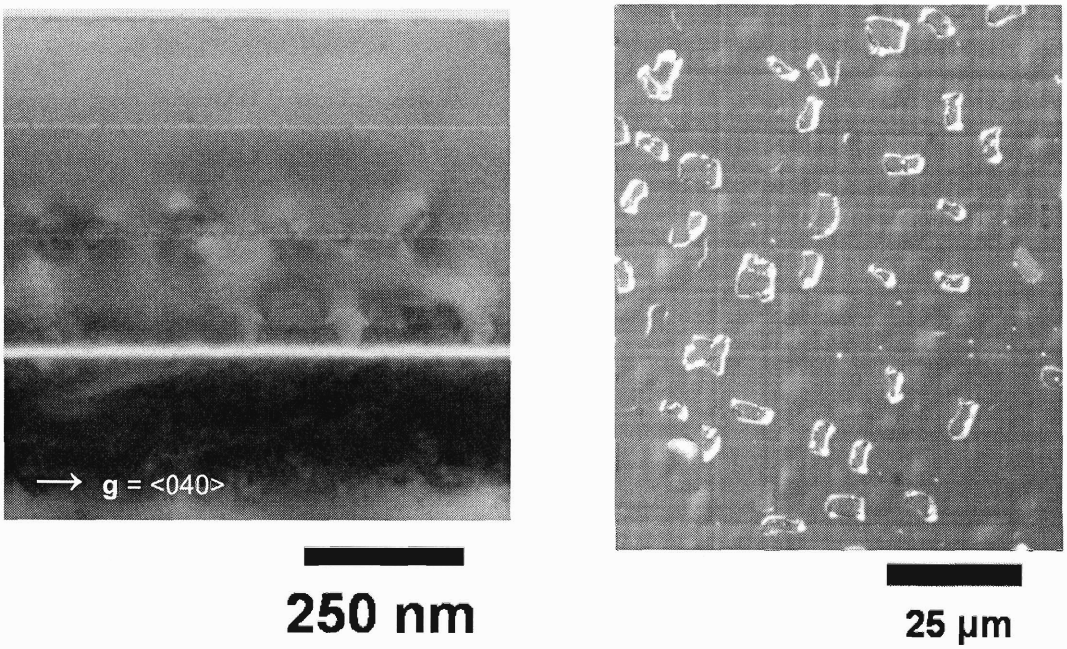


FIGURE 7.15 – (a) XTEM micrograph and (b) Nomarksi optical micrograph of the 50%-based structure after blistering. Note that the XTEM image in (a) is along the [110] pole.

The origins of the discrepancy in the exhibited splitting behavior of the various samples may lie in inherent differences in the implant damage resistance of the Si/SiGe system. It is well-known that SiGe alloys will preferentially amorphize over Si layers during ion implantation. (*110-114*) While much of this early work involved implanted superlattices consisting of alternating relaxed Si / compressively strained SiGe layers, the mechanism for the preferential amorphization of SiGe alloys over pure Si is now known to be due to the presence of Ge, and not the presence of compressive strain. (*112*) Thus, while tensile strain can serve to locally increase the solubility of H and allow for significant H-gettering to occur, the hydrogen ion implantation process itself may also serve to preferentially damage the surrounding relaxed SiGe matrix relative to the intended strained-Si gettering layer. As implant damage is a primary catalyst for the nucleation of hydrogen platelets, such damage in the surrounding SiGe matrix could result in a competing path for hydrogen accumulation and, as

such, a competing path for splitting and layer exfoliation, such as was observed in the splitting behavior of the $Si_{0.75}Ge_{0.25}$-based structure.

In order to test this hypothesis, Rutherford backscattering spectrometry (RBS) was performed to measure the relative damage in each of the previously characterized $Si_{1-x}Ge_x$ structures as well as a Si(001) wafer as a control. RBS spectra were acquired for each structure in both random as well as [100]-oriented channeling conditions in order probe the extent of the damage in the implanted regions. Each sample was tested in both the as-grown condition as well as after implantation and post-annealing at 300°C for 1 hour. Shown in **Figures 7.16-7.19** are the spectra for each $\nabla_x[Si_{1-x}Ge_x]$/Si-based donor structure as well as a simultaneously implanted Si(001) reference sample.

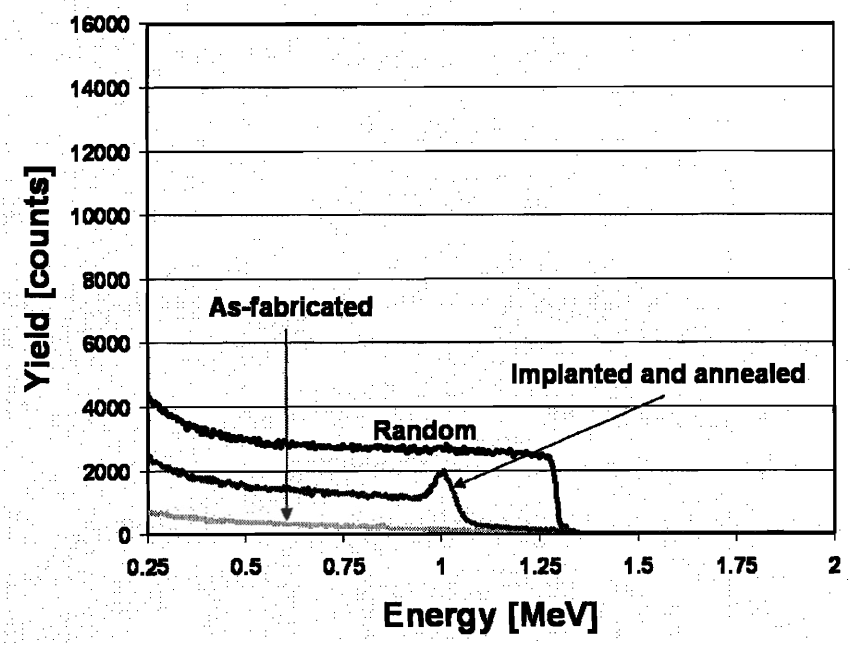


FIGURE 7.16 – RBS/ion channeling spectra of the Si reference sample in both the as-received and post-annealed conditions.

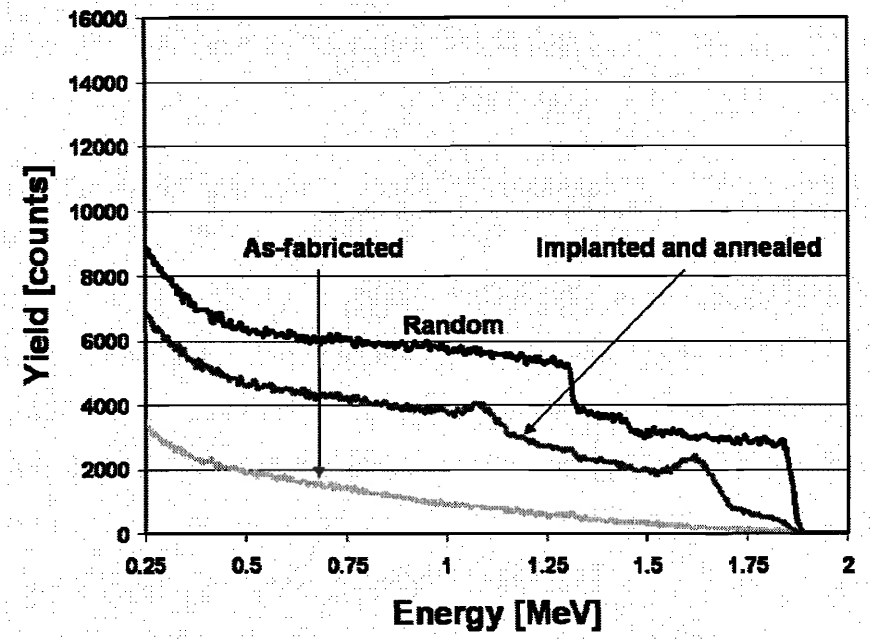


FIGURE 7.17 – RBS/ion channeling spectra of the $Si_{0.75}Ge_{0.25}$-based sample in both the as-grown and post-annealed conditions.

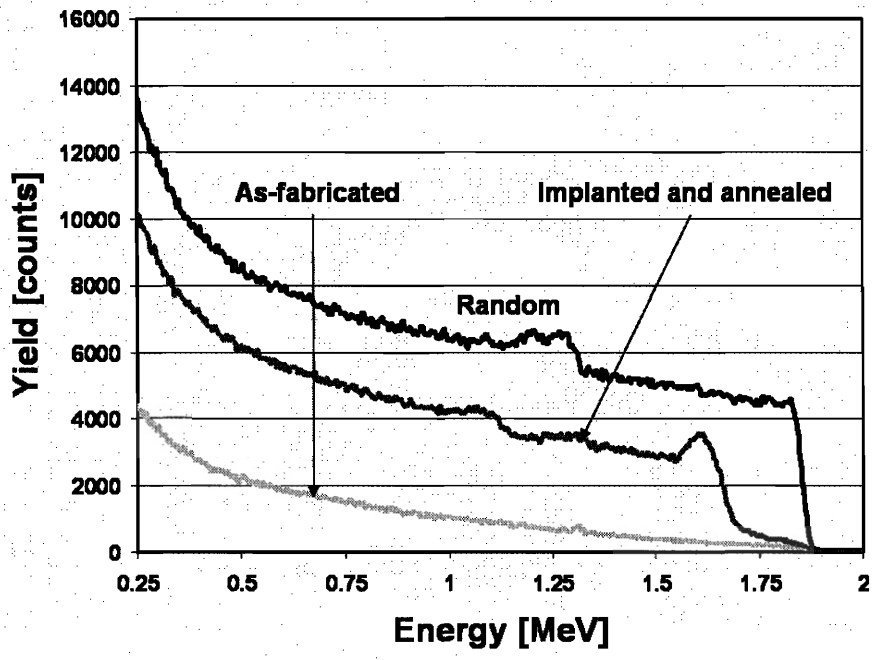


FIGURE 7.18 – RBS/ion channeling spectra of the $Si_{0.60}Ge_{0.40}$-based sample in both the as-grown and post-annealed conditions.

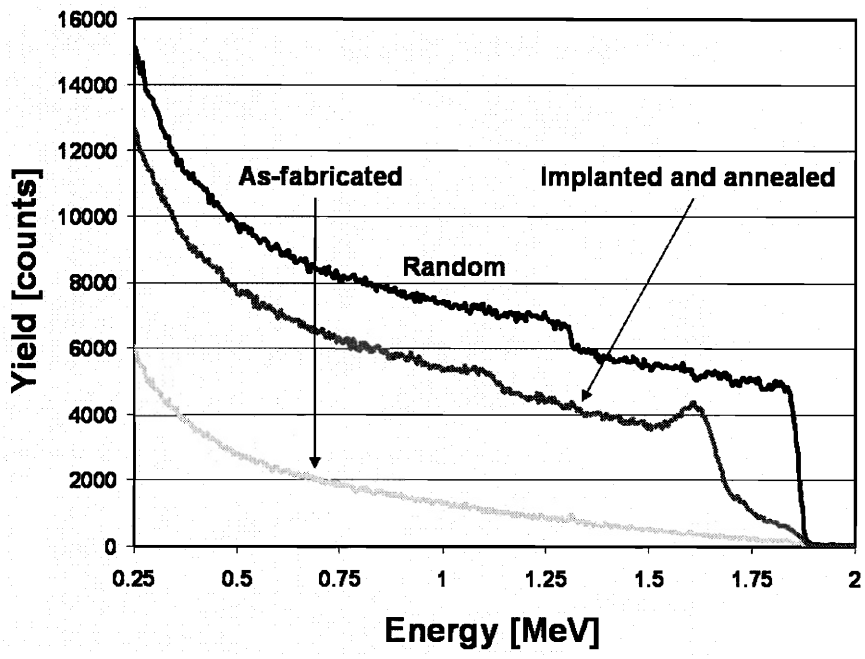


FIGURE 7.19 – RBS/ion channeling spectra of the $Si_{0.50}Ge_{0.50}$-based sample in both the as-grown and post-annealed conditions.

In order to quantitatively compare the damage profiles within each structure, a metric we refer here to as the *dechanneling fraction* was utilized. This quantity was defined as the ratio of the sum of the counts under channeling conditions to that of the sum of the counts of the random spectra. These counts were totaled within a 200keV energy window centered around the damage peaks of both Si and Ge. These data were then plotted for each structure as a function of their respective Ge concentrations, along with the strain induced in a Si layer by their respective $\nabla_x[Si_{1-x}Ge_x]$/Si buffers. These data are presented in **Figure 7.20**.

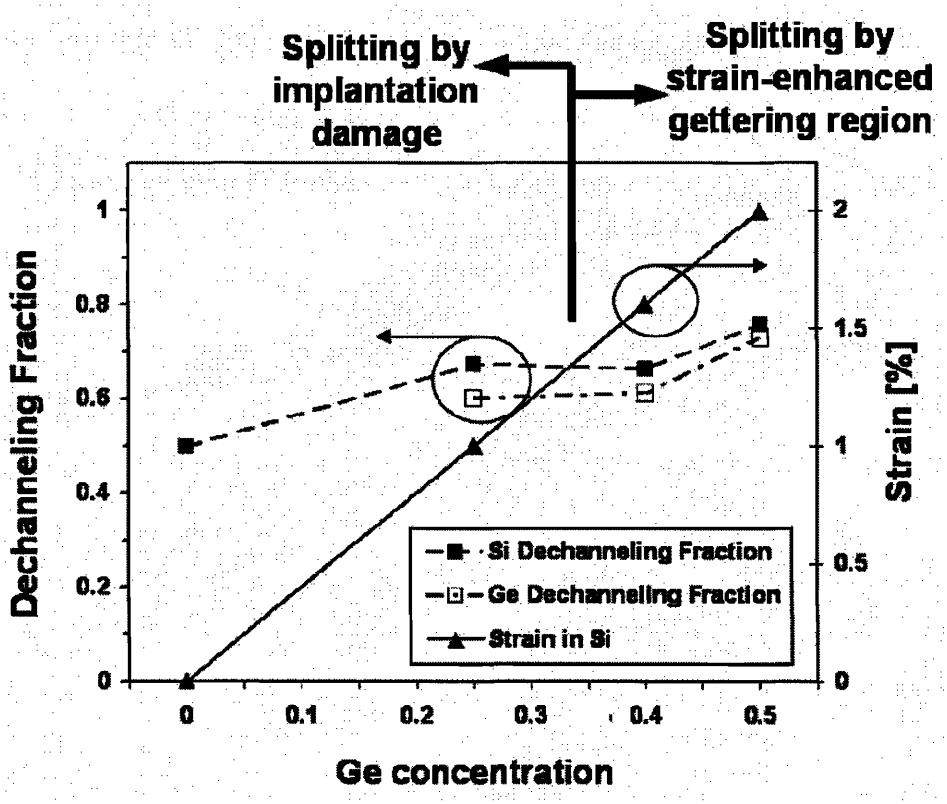


FIGURE 7.20 – Plot of the dechanneling fraction in the damaged region as a function of Ge composition in the surrounding structure. Shown at right is the strain induced in a Si layer as a function of Ge composition.

Thus, it can be seen from **Figure 7.20** that while the strain induced in a Si layer increases linearly with the final Ge concentration in the graded buffer, the damage induced during implantation increases sub-linearly. As a result, there are two regimes in the utilization of strained-Si layers for enhancing layer transfer using $\nabla_x[Si_{1-x}Ge_x]$/Si-based donor structures. In the low Ge concentration regime, i.e. $x_{Ge} \leq 0.25$, the strain induced in Si layers was found to be insufficient to result in significant H-gettering. However, the presence of Ge in the surrounding SiGe regions results in enhanced damage within the implanted region. Thus, while the H-content can be somewhat higher within the strained-Si layer than the surrounding SiGe regions, as was in fact shown in **Figure 7.6**, splitting can actually occur in neighboring SiGe regions which have more damage, as was shown in **Figure 7.13(a)**. In contrast, for greater Ge concentrations (i.e. $x_{Ge} \geq 0.4$), the strain induced in Si continues to increase thereby resulting in the

markedly increased local H concentrations in the strained-Si gettering layers exhibited in **Figures 7.7** and **7.8**.

As seen in **Figure 7.20**, however, the dechanneling fraction values, i.e. damage, in the surrounding SiGe regions for the $Si_{0.6}Ge_{0.4}$- and $Si_{0.5}Ge_{0.5}$-based samples are not significantly higher than that of the $Si_{0.75}Ge_{0.25}$-based sample. This is the root cause of the disparity between the splitting behavior exhibited by the 25- and the 40-/50% Ge samples. It is our belief that while the 1% tensile strained-Si sample did show a slightly enhanced H concentration relative to the surrounding $Si_{0.75}Ge_{0.25}$ layers, a higher level of damage in the surrounding $Si_{0.75}Ge_{0.25}$ actually allowed for preferential crack formation within the surrounding $Si_{0.75}Ge_{0.25}$ layers. In the $Si_{0.6}Ge_{0.4}$- and $Si_{0.5}Ge_{0.5}$-based structures, however, the strain induced in the Si layers was sufficient to allow for enhanced H-gettering to the extent that crack formation occurred along the lowest strained-Si layer, as intended.

Thus, when utilizing buried strained-Si layers in relaxed SiGe for layer exfoliation purposes, there are two regimes for splitting. In the low Si strain / high SiGe damage regime, splitting occurs in the surrounding SiGe layers due to preferential implantation damage, while in the high Si strain / high SiGe damage regime, splitting occurs within the strained-Si layers due to the emergence of preferential damage from strain-enhanced H-gettering. This strain-enhanced damage was shown to be in the form of the {100}-type platelets which form after proton implantation and annealing.

7.8 PRELIMINARY RESULTS FOR DONOR STRUCTURE RE-USE

In the previous section, strained-Si layers were shown useful for enhancing the layer exfoliation process when tensile strain levels met or exceeded 1.6%. While the use of such layers will likely prove useful for making SSOI substrate fabrication more economical through a reduction in the H^+

implantation dose, the issue remains that the original $\nabla_x[Si_{1-x}Ge_x]$/Si-based donor structure is typically discarded after fabrication of the engineered substrate, e.g. SSOI.

As shown above in **Figure 7.14**, the $Si_{0.6}Ge_{0.4}$-based experimental structure exhibited significant surface blistering when annealed at 300 °C for 1 hour followed by 1 hour at 500 °C owing to the preferential formation of cracks along the lowest strained-Si layer, i.e. the layer intended for splitting. For this reason, we chose this sample to demonstrate the re-use methods outlined above. As was shown in **Figure 7.14(b)**, the blistering process resulted in macroscopic flakes of material being separated from the $Si_{0.6}Ge_{0.4}$-based donor structure. If the structure is not rigidly bonded to another handle wafer, cracks can easily propagate to the free surface rather than continue parallel to the interface, i.e. the ideal direction of crack propagation. From the standpoint of the donor structure, however, this blistering process is functionally equivalent to the bonding and layer transfer process. (*106*) As such, the layer transfer process can be effectively modeled by selective chemical etching of the exposed strained-Si layer using a KOH solution. In this way, a KOH solution can be employed to chemically "split" the remaining exposed, damaged strained-Si layer in the same way that the mechanical splitting process would occur during a conventional hydrogen-induced layer transfer process. A cross-sectional TEM micrograph and a Nomarski optical image of the $Si_{0.6}Ge_{0.4}$-based experimental structure after blistering and subsequent KOH etching are shown in **Figure 7.21**.

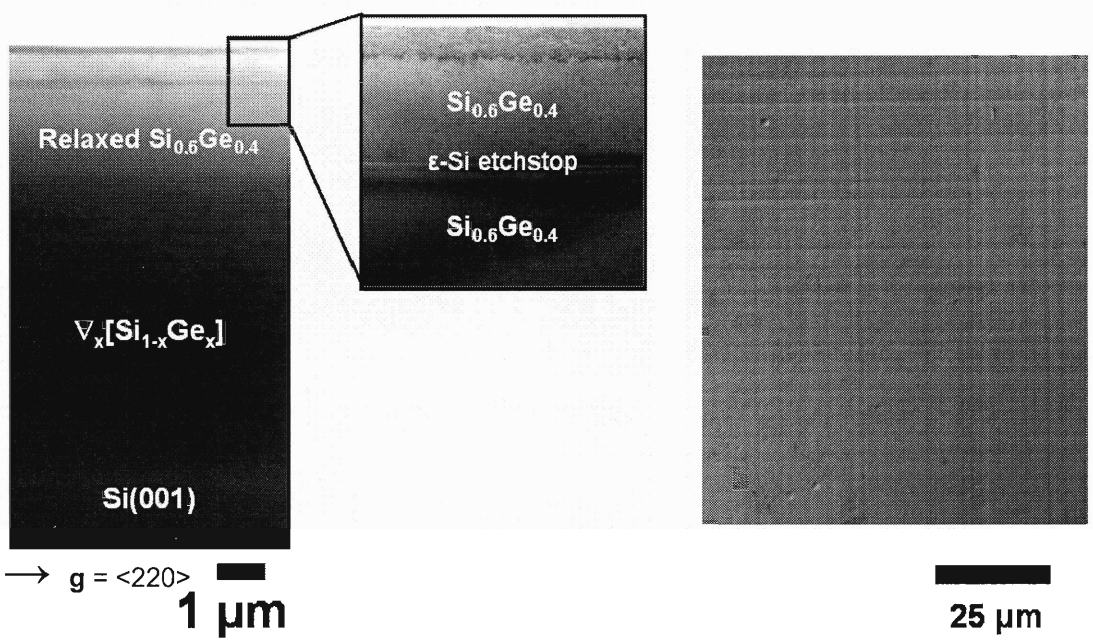


FIGURE 7.21 – (a) Cross-sectional TEM micrograph and (b) Nomarski optical image of the experimental $Si_{0.6}Ge_{0.4}$-based donor structure after KOH-etching.

With layer transfer effectively modeled using KOH selective etching of the blistered structure, the next step in the potential reuse of the SSOI donor structure involved removing the remaining SiGe spacer material. The structure was subsequently etched with a SiGe selective etchant (HNO_3:HAc:dHF). (*69*) A cross-sectional TEM micrograph and Nomarski optical image of the structure after SiGe removal are shown in **Figure 7.22**.

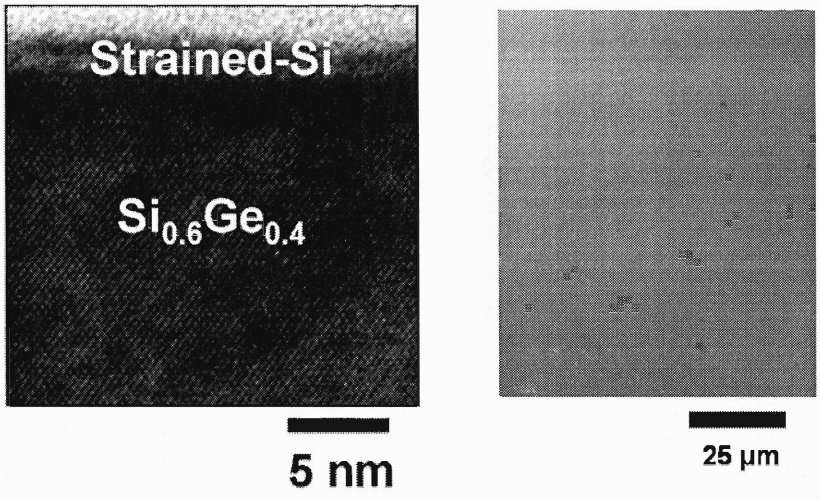


FIGURE 7.22 – (a) On-pole cross-sectional TEM micrograph and (b) Nomarski optical image of the experimental $Si_{0.6}Ge_{0.4}$-based donor structure after selective KOH- and SiGe-etching.

We note that in the state shown in **Figure 7.22**, the structure is identical to that shown in **Figure 7.3(d)**. As such, regrowth could theoretically proceed on the structure shown in **Figure 7.22**, thereby allowing a significant portion of the donor structure to be re-used. Accordingly, the overall cost structure of the initial Si substrate, relaxed graded buffer growth, and CMP step would reduce over time to first-order as *1/n*, where *n* is number of uses.

The methods presented in this section demonstrate potential for re-using a significant portion of SSOI donor structures. The methods described could also be employed for the fabrication of other types of engineered substrates, such as GOI, by utilizing an additional chemically-selective ε-$Si_{0.4}Ge_{0.6}$ layer beneath the ε-$Si_{0.4}Ge_{0.6}$ gettering layer.

7.9 CONCLUSION

Novel applications of strained-Si layers in $\nabla_x[Si_{1-x}Ge_x]$/Si-based donor structures for improving the fabrication of SSOI substrate were presented. Firstly, a method was presented whereby buried strained-Si layers can be utilized as

hydrogen gettering layers in SSOI donor structures. H-implanted strained-Si layers in relaxed SiGe with tensile strain levels of approximately 1.6% are required for sufficient hydrogen-gettering and concomitant platelet formation behavior to dominate the exfoliation process. Such strain levels in Si were necessary to have strain-enhanced gettering surmount the competing implantation damage that preferentially occurs in the surrounding relaxed SiGe alloy. Secondly, buried strained-Si layers were shown to have potential for allowing selective removal of the remaining damaged SiGe after layer transfer, thereby enabling a significant portion of the original $\nabla_x[Si_{1-x}Ge_x]$/Si-based donor structure to be re-used. Application of the principles presented in this work can be used to create a variety of engineered substrate materials.

CHAPTER 8: CONCLUSIONS AND SUGGESTIONS FOR FUTURE WORK

"All right, I'm gonna turn over the next card. Concentrate... I want you to tell me what you think it is."

- Dr. Peter Venkman

8.1 SUMMARY OF EXPERIMENTAL WORK

8.1.1 DEVIATIONS FROM IDEAL NUCLEATION-LIMITED RELAXATION IN HIGH-GE CONTENT RELAXED SIGE BUFFERS

The evolution of the TDD in relaxed graded SiGe buffers on Si ($\nabla_x[Si_{1-x}Ge_x]$/Si) was investigated in the high-Ge composition range, using the highest growth temperatures possible without the onset of gas-phase nucleation from the GeH_4 precursor gas used in this study. A significant rise in the TDD value was found as pure Ge was reached at 700°C. Similar to previous reports of Ge-rich bulk SiGe alloys, (*51*) this observation was attributed to mechanical weakening due to a loss of the solid-solution strengthening effect as pure Ge was approached. While this leads to significant dislocation nucleation at the temperatures desired for efficient strain relaxation, it was demonstrated that the dislocation nucleation in $Si_{0.02}Ge_{0.98}$ and Ge can be suppressed through a sufficiently reduced growth temperature. Thus, a transition from nucleation- to glide-limited relaxation during graded buffer growth was observed.

Furthermore, by coupling the grading and growth rates by growing at reduced growth rates for the same time as a 10 %Ge μm^{-1} reference, a drastic escalation in the threading dislocation density was observed. This is not due to a breakdown of the theoretical basis underpinning **Eqn. 4.1**, but rather the increased roughness induced by the combined effects of more intense strain fields due to higher grading rates and increased surface diffusion. This increased surface roughness leads to a progressive cycle of dislocation trapping and generation, which serves to further reduce the effective strain, ε_{eff}, locally on dislocations near pileups, thereby necessitating an increase in the TDD. In this way, it was shown that the key to obtaining thin, low TDD buffers centers around judiciously choosing grading and growing rates which allow for a high ε_{eff} value to be maintained, but neither of which is so high that rampant escalations in the

dislocation density are observed owing to excessively high strain application rates.

8.1.2 STRAINED-SILICON ON SILICON AND SILICON-GERMANIUM ON SILICON SUBSTRATE DEVELOPMENT

Two novel semiconductor platforms, strained-silicon on silicon (SSOS) and silicon-germanium on silicon (SGOS), were developed. SSOS substrate has an epitaxially-defined, strained silicon layer directly on bulk silicon wafer without an intermediate SiGe or oxide layer. PVTEM revealed a network of misfit dislocations with an average spacing of approximately 40 nm for this structure, corresponding to the full difference in lattice constant between 0.94% strained Si and relaxed bulk Si, respectively. SSOS substrate is interesting in that a *lack* of misfit dislocations would imply relaxation, in contrast with conventional strained heterostructures. The retention of strain implied by the array of edge dislocations at the interface, coupled to the fact that SSOS is entirely composed of silicon, makes this the first report of a *homochemical heterojunction*. Homochemical heterojunctions are a class of materials which exhibit bandstructure offsets due to differences solely in the strain state, not due to changes in composition as are conventionally achieved.

Silicon-germanium-on-silicon (SGOS) substrate utilizes a thin layer of SiGe to separate a strained-Si device channel from a bulk Si substrate. Specifically, this epitaxially-defined SiGe layer serves to distance the source and drain contacts from the interfacial array, thereby eliminating the off-state leakage problem SSOS would likely exhibit. Furthermore, by distancing the interfacial array from the overlying etching surface, preferential etching of dislocation is minimized, considerably simplifying substrate fabrication. Raman spectroscopy indicated that the transferred SiGe layer is fully relaxed, and therefore any strained-Si channel of sub-critical thickness on this platform would necessarily be fully strained.

8.1.3 ADVANCED DONOR STRUCTURES FOR SSOI AND SSOS SUBSTRATE FABRICATION

This thesis concluded with a study of utilizing buried ε-Si layers for improving the fabrication of SSOI, SSOS, and SGOS substrates via hydrogen induced layer exfoliation. Previous work involving tensile ε-$Si_{0.4}Ge_{0.6}$ layers in relaxed Ge/$\nabla_x[Si_{1-x}Ge_x]$/Si structures demonstrated that significant hydrogen gettering via the formation of strain-relieving platelets occurred within the tensile ε-$Si_{0.4}Ge_{0.6}$ layers, leading to an overall increase in layer transfer efficiency for GOI substrate fabrication. Tensile ε-Si layers in relaxed $Si_{1-x}Ge_x$, however, demonstrate markedly different hydrogen gettering behavior that is dependent on a combination of both the degree of tensile strain in the Si layer as well the amount of damage present in the adjacent SiGe layers. It was determined that tensile strained-Si layers in $\nabla_x[Si_{1-x}Ge_x]$/Si structures require approximately 1.6% strain to overcome preferential implantation damage in the relaxed SiGe cladding. Lastly, an advanced $Si_{0.6}Ge_{0.4}/\nabla_x[Si_{1-x}Ge_x]$/Si-based donor structure which incorporated ε-Si layers as transfer, gettering, and etchstop layers was demonstrated. Generalization of the features in this structure may prove useful for the reuse of significant portions of relaxed SiGe-based donor structures, thereby potentially speeding commercial adoption of engineered substrates such as SSOI, GOI, SSOS, and SGOS.

8.2 SUGGESTIONS FOR FUTURE WORK

8.2.1 $GeCl_4$ FOR REDUCED GAS-PHASE NUCLEATION

As described in **Chapters 3** and **4**, significant work went into growing at the highest possible temperature across the entire SiGe composition range in our UHVCVD reactor. While the growth temperature of the low Ge-content portion of graded SiGe buffer growth is limited by devitrification of the quartz tube as well as the o-ring cooling at the base of the reactor, the high Ge-content portion is

limited by the occurrence of gas-phase nucleation (GPN). This is primarily due to the GeH_4 gas precursor selected for the deposition of Ge-containing layers. Substitution of a Ge source gas with a reduced cracking efficiency, such as $GeCl_4$, would allow for higher growth temperatures in the mid- to high-Ge content portion of the graded buffer (i.e. $0.5<x_{Ge}<0.9$), thereby providing enhanced glide kinetics and potentially lower dislocation densities over this composition range. While the use of chloride-containing precursors is highly undesirable from a standpoint of reactor maintenance (especially true in an academic research environment), substitution of $GeCl_4$ for GeH_4 holds the greatest promise for reducing the dislocation density in the Fitzgerald group UHVCVD reactor up to approximately 90% Ge. Beyond approximately $Si_{0.1}Ge_{0.9}$, dislocation nucleation effects would likely come into play at 900°C (similar to the case of Ge at 700°C described in **Chapter 4**).

8.2.2 PATTERNED HANDLE WAFERS FOR IMPROVED SSOS/SGOS SUBSTRATE FABRICATION

Hydrophobic bonding is typically plagued by the formation of interfacial H_2 bubbles. These bubbles form after bringing the wafers into contact and annealing and are a direct result of hydrogen desorption from the H-terminated bonding surfaces. While the solubility of H is quite low in Si at typical bonding temperatures, the diffusivity of H is orders of magnitude greater along the bonded interface than through bulk Si. As a result, H will diffuse and agglomerate in the form of interfacial bubbles. This phenomenon was likely the primary factor which limited the transfer efficiency in SSOS and SGOS substrate fabrication. Recently, results on the fabrication of SSOS have been presented which circumvent this problem by transferring thin slabs of strained-Si to Si handle wafers with widths on the order of 10μm. (*115*) Transfer of a blanket layer with this approach, however, is not possible.

One means of transferring blanket Si films to Si while simultaneously controlling the formation of bubbles involves the use of Si handle substrates with pre-etched channels.(*116*) Results of this study are shown in **Figure 8.2**.

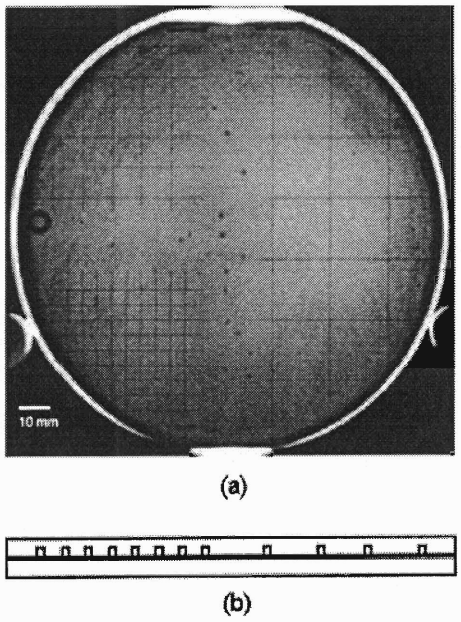


FIGURE 8.1 – (a) Hydrophobically-bonded Si wafer pair with etched grid at interface and (b) cross-sectional schematic of bonded pair. Image courtesy of Esser *et al*. (*116*)

The patterned substrates aid hydrophobic Si-Si bonding by providing a means through which hydrogen released from the bonded interface can diffuse out of the structure. In this way, hydrogen is released from the bonding surfaces and diffuses along the bonded interface to the channels, where gaseous hydrogen eventually leaves the structure entirely. This leaves Si-Si bonds across a bubble-free interface, assuming the distance between the channels is less than the effective diffusion distance of hydrogen along the interface. While the presence of the channels reduces the effective area transferred, the increase in yield due to the reduction in interfacial bubbles more than offsets this drawback.

8.2.3 TENSILELY STRAINED SiGE LAYERS FOR IMPROVED H-GETTERING EFFICIENCY

As demonstrated in **Chapter 7**, Si layers with approximately 1% tensile strain did not result in sufficient H-gettering to demonstrate preferential crack formation, while Si layers with 1.6% and 2% tensile strain showed remarkably preferential crack formation. This observation was attributed to the fact that sufficient strain was required to offset the relatively high damage rates in the adjacent SiGe layers. One possible way to overcome this shortcoming would be to explore low-Ge content tensilely strained H-gettering layers. For example, a ε-$Si_{0.95}Ge_{0.05}$ layer in relaxed $Si_{0.70}Ge_{0.30}$ will have the same level of tensile strain as a ε-Si layer in relaxed $Si_{0.75}Ge_{0.25}$, however the difference in implantation damage rates between $Si_{0.95}Ge_{0.05}$ and $Si_{0.70}Ge_{0.30}$ may be smaller than Si and $Si_{0.75}Ge_{0.25}$.

8.2.4 STRAINED-SILICON ON LATTICE-ENGINEERED SUBSTRATE (SSOLES)

For various reasons, leading-edge Si fabs are reluctant to allow entry to III-V materials such as GaAs. One solution to this problem currently under development in our group is silicon on lattice-engineered substrate (SOLES). SOLES provides a surface SOI layer for the fabrication of microelectronic devices as well as an easily accessible (e.g. through selective etching) high-Ge template for the growth of III-V optoelectronic devices such as lasers. Since the surface of this structure is composed of Si, it is expected that the barrier to entry into a leading-edge Si fab will be minimal. As shown in **Figure 8.2**, the Si and high-Ge content layers are nearly coplanar. The close proximity of the layers drastically facilitates the integration potential for devices on each template.

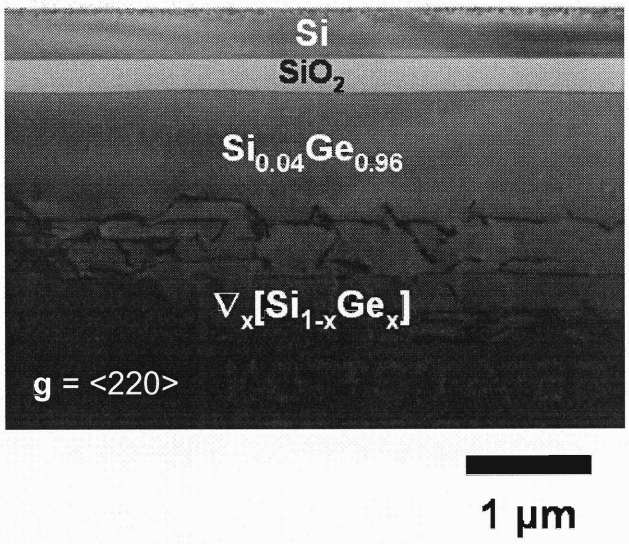


FIGURE 8.2 – XTEM micrograph of a silicon on lattice-engineered substrate (SOLES) structure. Image courtesy of C. L. Dohrman. (*117*)

While the SOLES structure shown in **Figure 8.2** has incredible promise for integrating microelectronic and optoelectronic devices, an alternative embodiment could involve the transfer of a thin strained-Si layer to create a surface SSOI layer. This strained-silicon on lattice-engineered silicon (SSOLES) structure could be cost-effectively fabricated, for example, using the re-useable $Si_{0.6}Ge_{0.4}$-based donor structure developed in **Chapter 7**. Such an advanced structure would integrate high-mobility CMOS devices as well as III-V devices on the same platform.

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